Co-planar waveguides for microwave atom chips

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by

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Abstract

This thesis describes research to develop co-planar waveguides (CPW) for coupling microwaves from mm-scale coaxial cables into 50 μm-scale microstrip transmission lines of a microwave atom chip. This new atom chip confines and manipulates atoms using spin-specific microwave AC Zeeman potentials and is particularly well suited for trapped atom interferometry. The coaxial-to-microstrip coupler scheme uses a focused CPW (FCPW) that shrinks the microwave field mode while maintaining a constant 50 Ω impedance for optimal power coupling. The FCPW development includes the simulation, design, fabrication, and testing of multiple CPW and microstrip prototypes using aluminum nitride substrates. Notably, the FCPW approach may be useful in concentrating the microwave near field to increase its coupling with co-located ultracold rubidium atoms to generate spin-squeezing.

Chapter 1

Introduction

1.1 Physics Motivation

This project studies microwave transmission in a co-planar waveguide (CPW) to support the development of an atom interferometer on a microwave atom chip. To this end, the project focused primarily on developing efficient coupling of microwaves into an atom chip using focused CPW (FCPW) transmission lines. In the longer term, these FCPW structures can potentially be used for enhancing atom-microwave coupling to generate spin-squeezing. The Aubin Lab is developing an atom interferometer based on spin-dependent microwave atom traps on an atom chip. This atom chip should be robust under frequencies of up to 20 GHz, so initial prototype tests need to meet efficacy standards of impedance-matching up to about 10 GHz. This setup is compact and will potentially possess a long phase integration time for extra sensitivity. Atom interferometers, much like optical interferometers, rely on the interference of, and phase shift between, two atomic paths. Atomic interferometers are even more sensitive than their optical counterparts, and use atomic matter waves that follow two such paths, generating an interference pattern highly sensitive to minute energy differences between the two paths. An atom interferometer can precisely measure changes in electric and magnetic fields, gravitational variations, and surface and inertial forces.

One challenge of atom chip interferometry is efficient insertion of microwaves onto the small atom chip, as the inserted microwaves must be impedance-matched with the atom chip to avoid reflections. There is also an opportunity to minimize the quantum projection noise, or shot noise, of the interferometer via spin-squeezing, a quantum entanglement scheme that can improve the precision and sensitivity of the interferometer. The FCPW may be useful in generating this effect, though other avenues are available for consideration as well, such as spin-squeezing in the vicinity of an optical nanofiber or via atom-atom interactions.

1.2 CPW-based cable-chip coupler

The CPW is a promising solution to the microwave insertion problem, as it effectively guides microwaves to an atom chip. The traditional CPW has a straight conducting center copper trace, but this project requires a modified CPW with a tapered trace to guide the microwaves from a larger source trace to a smaller output trace. The FCPW is comprised of an Aluminum Nitride (AlN) substrate, a center trace, top and bottom ground planes, and metallic vias to connect the ground planes and constrain the microwave field to the center trace (tapered to provide focusing, while impedance is kept constant). Figure 1.1 shows a standard CPW copper transmission line (left), as well as the focused CPW transmission line (right).

The FCPW acts as a microwave coupler that carries and focuses microwaves from a coaxial cable source to insert them into the atom chip's microstrip transmission lines. As the atom chip's microstrip transmission lines are 54 microns wide, the coupler's key component is its focused CPW (FCPW) transmission line that focuses the large microwave field mode of the coaxial cable (mm-scale) into a size compatible with the atom chip (μm-scale).

Development of the coax-to-FCPW-microstrip coupler system requires the design

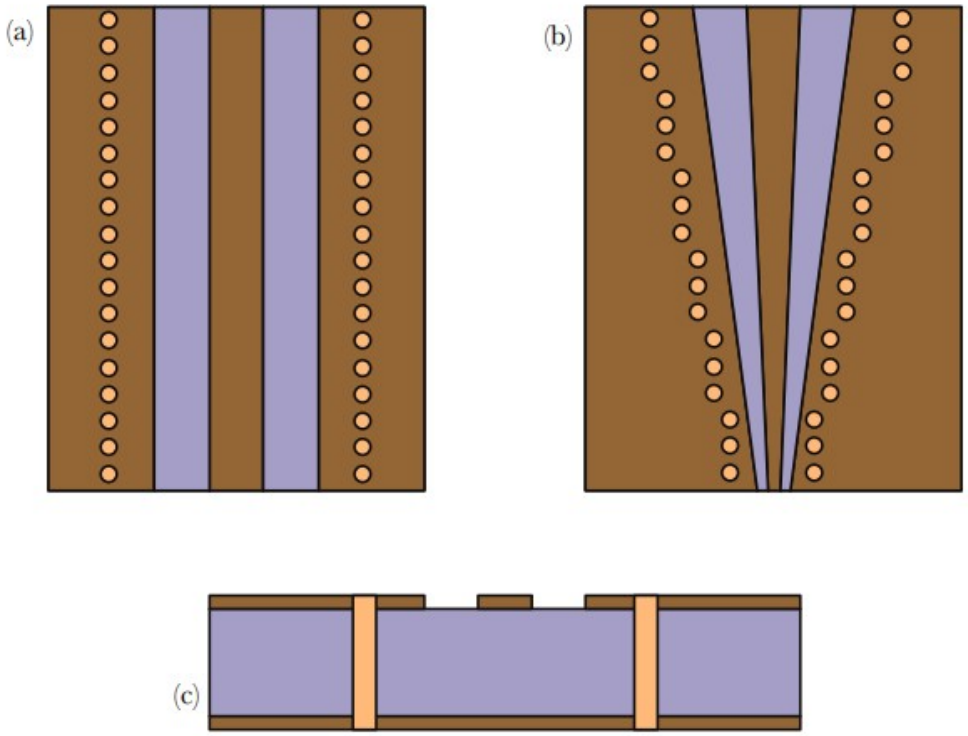

Figure 1.1: **CPW Geometries**: In figures (a-c), components of thin copper plating are brown, aluminum nitride (AlN) substrates are lilac, and copper vias are orange. Dimensions not to scale. (a) Top view of a standard CPW, consisting of a center copper trace and two top ground planes on an AlN substrate. Small metal vias connect the top ground planes to the bottom ground plane (not visible). (b) Top view of focused CPW, with a tapered center trace. The top groundplanes are tapered to maintain 50 Ohm impedance, and the vias are piecewise tapered and connect to the lower groundplane (not visible). (c) Side view of a CPW, showing the top groundplanes connected to the lower groundplanes through the substrate by vias on either side of the trace.

and simulation of both the coaxial cable and FCPW together, as well as simulations to test the effectiveness of the FCPW-to-microstrip sub-system. Indeed, thorough testing of FCPW performance requires prototype construction using a PCB board to test the behavior of microwaves sent from a coaxial cable to the PCB prototype, and finally into a microstrip.

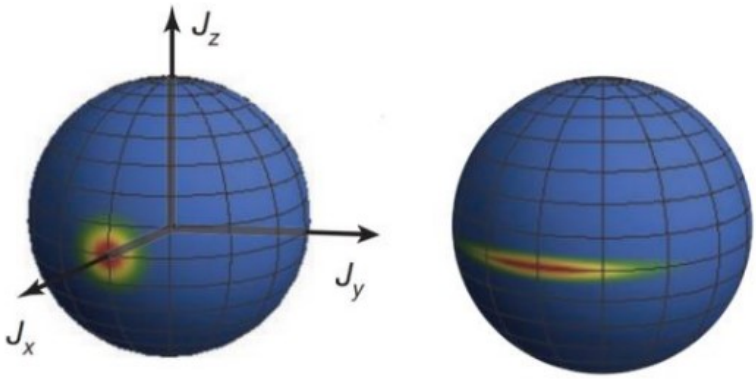

Figure 1.2: **Bloch Spheres:** Two Bloch spheres show uncertainty in the total spin $\vec{J}$ components of (x,y,z). Depicted are Bloch spheres with no spin-squeezing (left) and spin-squeezing along $\vec{J}_z$ (right). Figure adapted from Hosten et al, Nature 2016 [1].

1.3 Further Motivation: FCPW generation of spin-squeezing

Traditionally, the two modes or paths in an interferometer do not interact, and thus function using only single-particle physics. In the case of a spin-dependent interferometer, as in the one this project will support, the interference of the two modes leads to two possible outcomes for the spin, spin up or spin down, upon detection of an atom. Any atom existing in an equal superposition of these two states must then choose between them (similar to a coin toss), leading to quantum projection noise, or shot noise, if the atoms are uncorrelated. Correlated modes, i.e. spin-squeezed modes, however, have been shown to reduce the shot noise in the system by a significant factor (i.e. the coin will "try" to come up heads as often as tails, not leaving this process just to chance), improving the overall precision and sensitivity of the interferometer.

The spin components of a particle obey a Heisenberg uncertainty principle, i.e. permitting uncertainty in one component can allow much lower uncertainty in another. For example, in a spin-$\frac{1}{2}$ system, the spin components of the total spin $\vec{S} = (S_x, S_y, S_y)$

obey the following uncertainty relations:

$$\Delta S_x \Delta S_y \geqslant \frac{\hbar^2}{4} \quad \text{and} \quad \Delta \vec{S}_y \Delta S_z \geqslant \frac{\hbar^2}{4} \quad \text{and} \quad \Delta S_z \Delta S_x \geqslant \frac{\hbar^2}{4} \tag{1.1}$$

where $\Delta \vec{S}_i$ is the uncertainty in the spin along the associated axis (with $i = (x, y, z)$) and is given by

$$\Delta \vec{S}_i = \sqrt{< S_i^2 > - < S_i >^2} \tag{1.2}$$

In a system with N identical spins there are similar uncertainty relations for the total spin $\vec{J} = \sum_{n=1}^{N} \vec{S}_n$:

$$\Delta \vec{J}_x \Delta \vec{J}_y \geqslant \frac{\hbar^2}{4} \quad \text{and} \quad \Delta \vec{J}_y \Delta \vec{J}_z \geqslant \frac{\hbar^2}{4} \quad \text{and} \quad \Delta \vec{J}_z \Delta \vec{J}_x \geqslant \frac{\hbar^2}{4} \tag{1.3}$$

By introducing correlations between atoms, the uncertainty can be increased in one component and decreased in another, thereby reducing shot noise upon measuring the reduced-uncertainty component. Figure 1.2 illustrates this interplay between components J_x and J_z on a spin Bloch sphere, where one shows no squeezing (left) and the other shows squeezing of J_z at the expense of J_x (right).

Already, correlated (spin-squeezed) modes have been successfully created using a cavity [1,2], yielding sensitivity improvements on the order of 10-100. In an FCPW, the microwave magnetic field strength depends inversely on the trace width, thus increasing the atom-microwave coupling significantly, i.e. the effect that one microwave photon has on an atom. While spin squeezing is not the main motivation for the developing an FCPW transmission line, it is a potential spin-off application of this work.

1.4 Structure of Thesis

This thesis is structured in the following manner: Chapter 2 provides a brief overview of the microwave atom chip, including its use of the AC Zeeman effect for atom trapping and interferometry, as well as the basic physics of CPW transmission lines. Chapter 3 describes simulation and design of the various CPWs that culminated in the final FCPW model, including discussion of noise reduction techniques and simulation results for comparison with prototypes. The prototypes are then described in Chapter 4, along with the entire testing process from quality control to soldering. Chapter 5 then details the results of impedance tests performed on the prototypes.

Chapter 2

Theory: Microwave atom chips for atom interferometry

2.1 Atom Interferometry

Atom interferometers, devices that make precise measurements of forces and potentials, have significant advantages over optical interferometers and other precision measurement devices. Like their optical counterparts, they rely on a wave following two paths simultaneously and the measurement of an induced phase difference between the paths of the waves. Atom interferometers thus require conditions that allow atoms to be measured as waves, such as in a Bose-Einstein Condensate (BEC), where atoms exhibit quantum properties at temperatures approaching 0 K. In spin-dependent interferometry, each atom is put into a superposition of spin-up and spin-down, with each spin component following a different path.

Trapped-atom interferometry yields an additional advantage to many modern interferometers: the atoms are localized, thus enabling a potentially small apparatus. Furthermore, with trapped atoms, the interferometer can have a long phase integration time, during which measurements can be made with increasing precision.

2.1.1 AC Zeeman Effect

The main atom chip for the interferometer relies on microwaves to create the atom trap. The rubidium atoms used in the experiment have a spin up state and a spin down state which are separated by some energy E that corresponds to a frequency $\omega_{\uparrow\downarrow}$ (i.e. with $E = \hbar\omega_{\uparrow\downarrow}$) . If the microwave frequency ω differs from $\omega_{\uparrow\downarrow}$, the frequency difference between them is known as the detuning δ with $\delta = \omega - \omega_{\uparrow\downarrow}$. Depending on the sign of δ and the spin state, the atoms become high-field or low-field seekers, i.e. an atom is attracted toward a region of high microwave intensity or repelled by it.

The detuning affects the energy difference between the two states: if δ is negative (microwave frequency is smaller than the original energy gap) then the energy gap widens; if δ is positive (microwave frequency is larger than the original energy gap) then the energy gap decreases, as shown in Figure 2.1. Since an atom seeks out the lowest energy configuration, if an atom's energy level is now higher, it becomes a low-field seeker; an atom whose energy level is now lower becomes a high-field seeker. Thus producing maxima (high fields) or minima (low fields) in electromagnetic fields should produce successful atom traps, by attracting all atoms of the same spin state to the same place.

2.1.2 Microwave Atom Chip

Combining the microwave fields generated by neighboring microstrip traces on the atom chip, which is shown in Figure 2.2, produces a microwave magnetic minimum, and low-field seekers are trapped in this minimum. This minimum is at the center of the near field diagram in the simulation shown in Figure 2.2, and power and phase adjustments in the input microwaves allow left-right and up-down control of the trap.

The coaxial cable from the microwave source is much larger than the center trace on the atom chip, where the microwaves must be inserted. Coupling between the two is highly ineffective, so an intermediary “adapter" is required for effective microwave

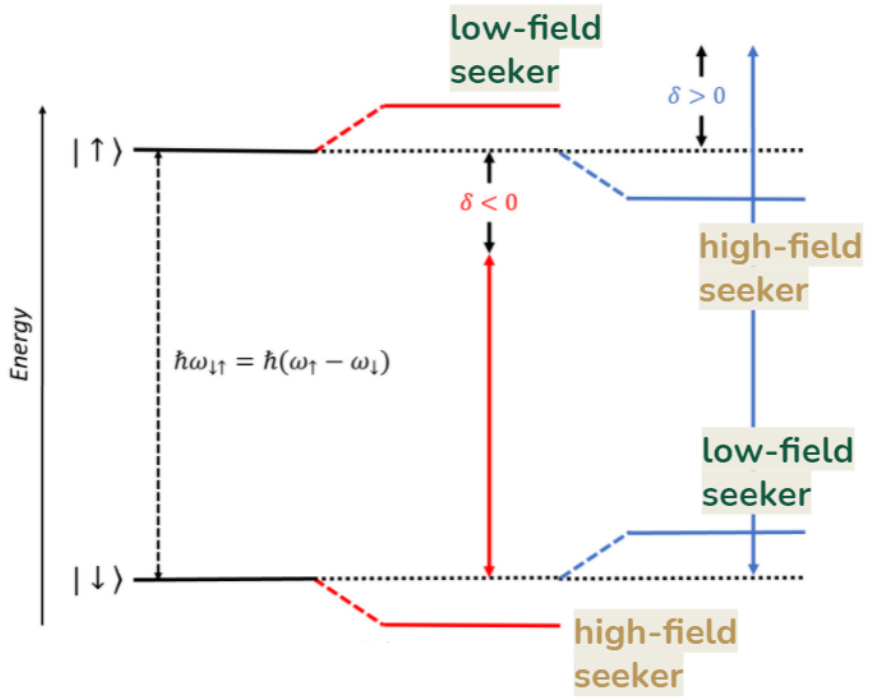

Figure 2.1:
AC Zeeman Effect: Depicted is an energy diagram for two states, spin up $|\uparrow\rangle$ and spin down $|\downarrow\rangle$ separated by some energy that corresponds to a frequency difference $\omega_{\uparrow\downarrow}$. If this two-level system interacts with a microwave of a different frequency ω then the difference is given by a detuning δ that either widens the energy gap (red) or closes the energy gap (blue) between the two states. Figure adapted from Miyahira et al, as presented at DAMOP Conference 2021.

insertion. Candidates for microwave insertion must have low reflection, consistently yield 50 Ω impedance, and be manufacturable.

2.2 CPW Calculations and Theory

The main components of a co-planar waveguide are the two conducting planes on top of the substrate, parallel to the center trace. The impedance of a CPW is determined by ratios between the height of the substrate h (and its chemical makeup), the width of the center trace s, the gap width between the center trace and the upper groundplanes w,

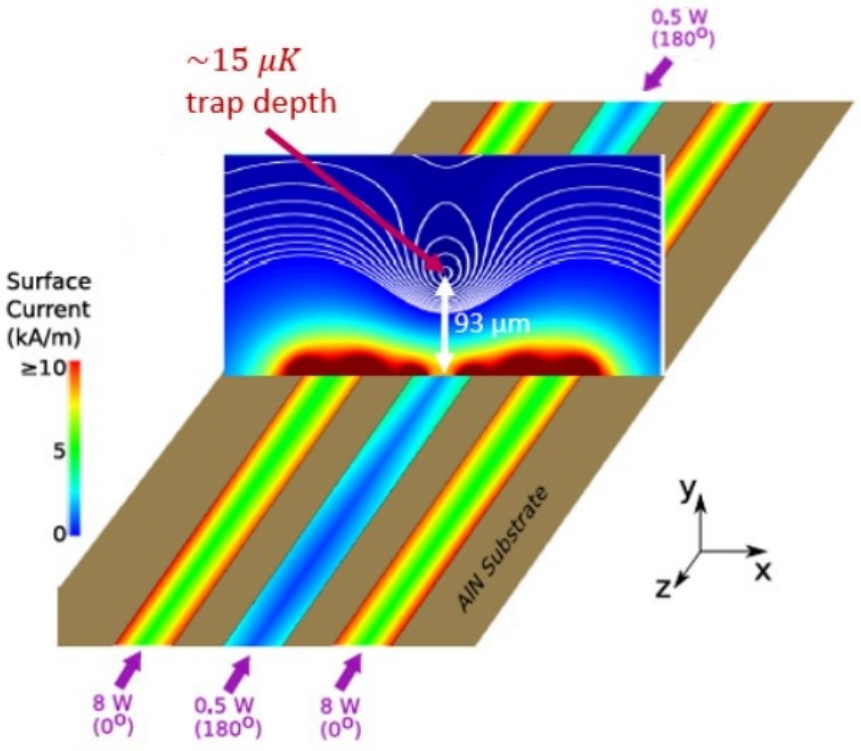

Figure 2.2: **Microwave Atom Chip**: The microwave atom chip used for trapping the atoms for use in interferometry is shown. Three center traces carry microwaves (the center trace is out of phase with the other two). The calculated near field diagram depicts the regions of high and low potential in red and blue respectively. The potential is for a ^{87}Rb atom driven at 6.8 GHz with a detuning $\delta = 2\pi \times 1$ MHz. Figure adapted from Miyahira et al, as presented at DAMOP Conference 2021.

as shown in Figure 2.3, as well as the dielectric constant ϵ that is unique to the substrate material.

The physical dimensions all contribute to the effective dielectric constant ϵ_{eff}, which determines the characteristic impedance through the CPW, based on electric field behavior in the substrate itself. Figure 2.4 depicts three different cases of CPW in which the electric field behavior influences the ϵ_{eff}. Qualitatively, these diagrams offer a prediction for the effective dielectric constant: The more the field lines are inside the substrate itself, the higher ϵ_{eff} will be. Conversely, the more the field lines are "above" the cop-

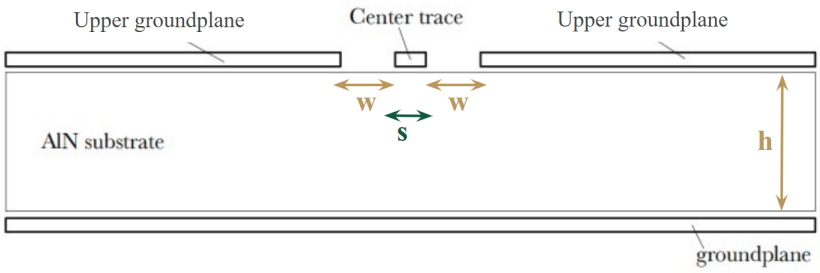

Figure 2.3: **CPW Side View**: Our Aluminum Nitride (AlN) substrate CPW is comprised of lower and upper copper groundplanes and a copper center trace. Here, s is the width of the center trace, w is the gap between the trace and the upper groundplanes on either side, and h is the height of the substrate.

per plating and outside of the substrate, the lower ϵ_{eff} will be. Diagram (a) will have a higher value compared with (b) and (c), since in (b) the lower groundplane is no longer producing a strong field with the trace, and in (c) the field lines are "raised" to produce a stronger field between the upper copper components.

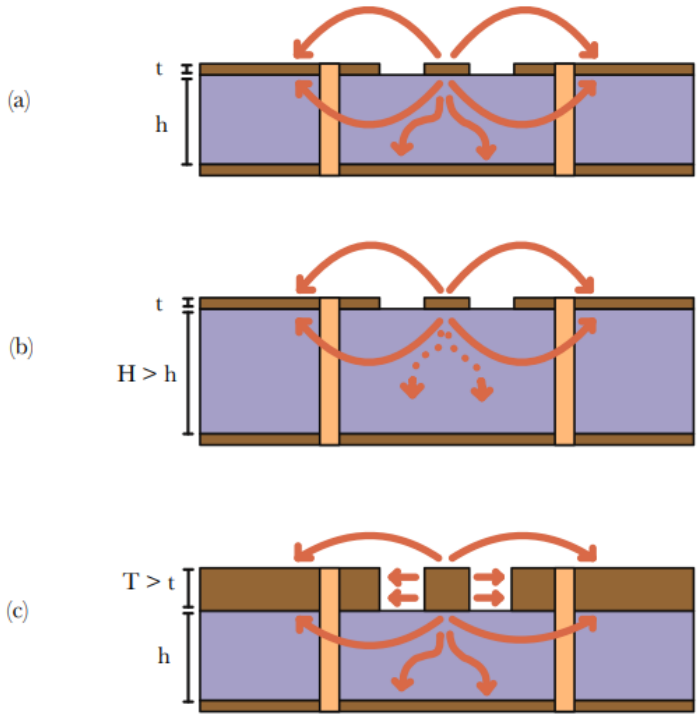

Figure 2.4: **CPW Electric Field Lines**: Diagrams (a-c) depict three co-planar waveguides with copper plating components (brown), vias (orange), and AlN substrate (lilac). All three are of constant trace width and gap width, but with varying copper thickness and substrate height. Electric field lines (red) are shown (for simplicity) from the microwave source on the center trace to the upper groundplanes and lower groundplane. (a) A typical CPW with copper thickness t and substrate height h is shown with electric field lines from the center trace to all three groundplanes. (b) A thicker substrate, of height $H > h$, with copper thickness t decreases the electrical connection to the lower groundplane. The field lines between the trace and upper groundplanes remains the same. (c) In a CPW of substrate height h and thicker copper thickness $T > t$, there is a stronger electric field between the trace and upper groundplanes laterally, and the lower groundplane is the same as the typical model.

Chapter 3

FCPW Development

3.1 FCPW Design

Design success is measured by simulated results of the reflection coefficient and the impedance for a wide range of microwave frequencies (typically 1-20 GHz, with a higher focus on frequencies below 8 GHz). Ideally, the reflection would be minimized– as close to 0 as possible, and the impedance graph would be centered around 50 Ω. CPW impedance is stable across a wide frequency range, making it an ideal choice for microwave insertion into the atom chip.

The development of an effective FCPW required that the impedance be kept constant. For ease of manufacture, the substrate height is kept constant and s and w are varied proportionally along the length of the trace. We investigated two methods of CPW tapering.

3.1.1 Traditional CPW

The CPW that we designed has an Aluminum Nitride (AlN) substrate, a lower groundplane, and two fences of Copper vias, shown in Figure 3.1. Vias are (often hollow) copper pillars that provide electrical connection from the upper groundplanes on either side of the center trace to the lower groundplane.

In initial simulations of CPWs, we found that high-frequency microwaves spill over

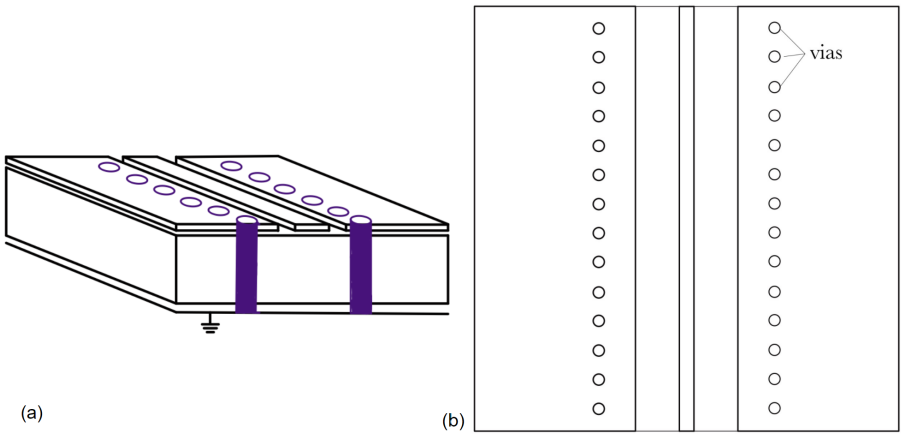

Figure 3.1: **CPWs with Vias** (a) A traditional CPW is depicted from the side: Two via fences (purple) run parallel to the center trace, about 0.8 mm from the edge of the gap. (b) Depicts a CPW from a top view: The via fences can be seen running along the length of the entire CPW.

into the upper groundplanes and reflect off the sides, creating an interference pattern on those groundplanes and harming the models' impedance and reflection performance. In order to contain the microwaves on the center trace, we added these two rows of vias about 0.8 mm from the inner edge of the upper groundplanes, as shown in Figure 3.1. Vias are copper pillars that run through the substrate, from the upper groundplanes to the lower groundplane, to provide additional grounding. These successfully ground any stray microwaves and protect the center trace from reflected waves.

3.1.2 Linear Taper

Our focused co-planar waveguide (FCPW) is essentially a series of CPW segments of decreasing center trace size on a single chip, as shown in Figure 3.2. The microwaves propagate from the wide end of the FCPW (which will connect to the coaxial cable acting as a microwave source) to the thin end of the FCPW (microwave output to the atom chip). This final thinnest segment matches the width of the traces on the microwave atom chip.

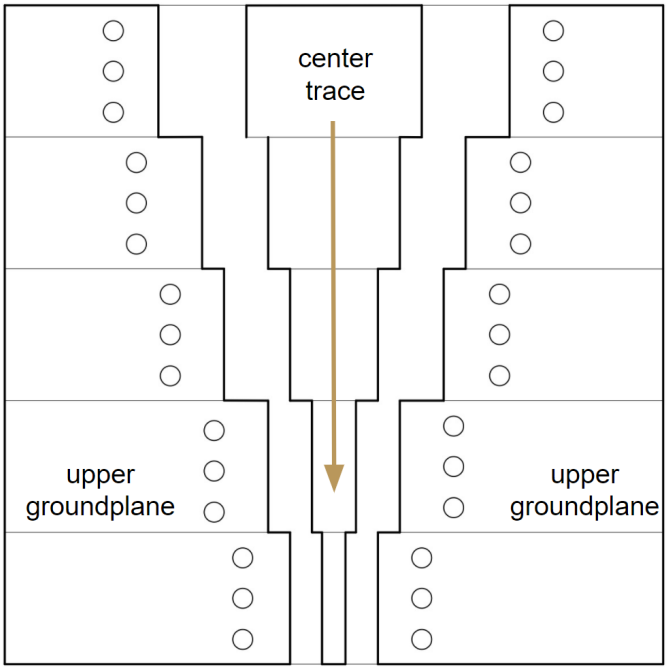

Figure 3.2: **FCPW Top View:** This example FCPW contains 5 segments that mimic regular, non-tapered CPWs: Each segment's ratio of gap width and trace width gives precisely 50 Ω impedance for a 1.00 mm substrate, such that the impedance is exact and consistent along the length of the FCPW. The center arrow indicates the direction of microwave propagation.

3.1.3 Trapezoidal Taper

The trapezoidal taper FCPW was developed next, in an attempt to reduce any reflections from the 90°angles present in the linear taper model. As shown in Figure 3.3, this model was comprised of a series of trapezoid trace segments (and their corresponding trapezoid upper groundplane segments). The software we used for modeling, FEKO from Altair Engineering Inc. [3], does not allow for a shape's edges to be defined by an equation, and so only the endpoints of the trapezoid were designed to yield 50 Ω impedance. The taper in between the endpoints was linear, leaving large portions of the taper dimensions as approximate, since the ratio of s to w is not linear.

Surprisingly, this model did not reduce reflection. In fact, the reflection coefficient

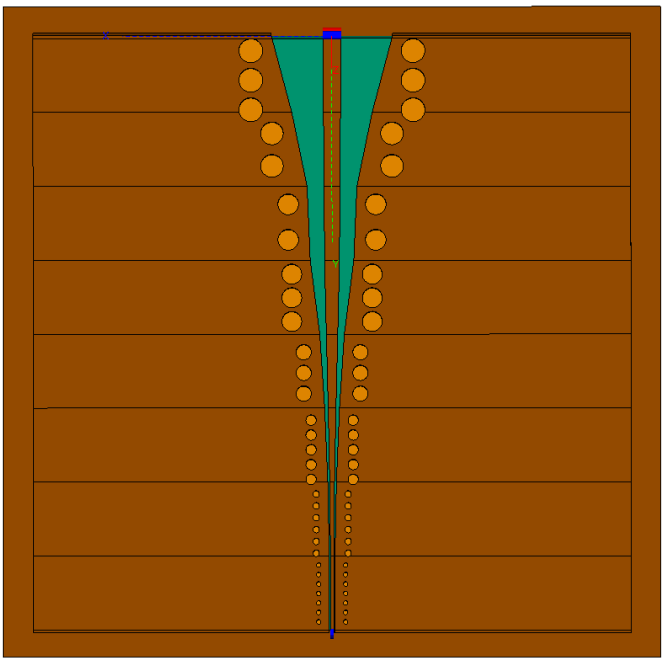

Figure 3.3: **FEKO Simulation of Trapezoidal FCPW:** Depicted is a FEKO model of a trapezoidal FCPW, in which a series of trapezoid trace segments and the corresponding trapezoid dimensions of upper groundplanes have been arranged in a taper.

was actually worse than with the linear taper. This is likely due to imprecise impedance matching, as poor coupling can cause reflection. Perhaps unsurprisingly, the impedance values did suffer tremendously, and this overall design was quickly dismissed.

3.2 Final Simulation Results and Canonical FCPW Model

After initial simulations were completed using Altair FEKO, the designs needed to be recreated using Sonnet Suites from Sonnet Software Inc. [4], which allowed for exporting the designs in a file format more compatible with typical manufacturer preferences, and it would also allow for verification of the simulation results. The two software tools which we used, however, calculated different average impedances for the same CPW dimensions. This discrepancy required investigation into the reliability of the software, as

Sonnet produces quick results and is more specialized to planar calculations, and FEKO is more thorough in 3D calculations and near field simulations. Both have been relied upon heavily throughout the CPW development process.

The two agree, however, in non-CPW chip simulations, indicating that the discrepancy was not due to the software themselves but in the production of the CPW model or setup.

3.2.1 Simulation Software Comparisons

The main difference between the Sonnet models and the FEKO models was in the thickness of the copper plating for the upper groundplanes and the center trace. In FEKO, the thickness was 0.005 mm, so this layer was approximated and built as a 2D plane. Since these models agreed with our impedance calculations for a 50 Ω CPW, we applied the same strategy to Sonnet models, though the thickness was now set to 0.035 mm (to model the thickness available for commercially manufactured prototypes).

In Sonnet, after changing the copper thickness to the new 0.035 mm thickness (but still approximating as a 2D plane), the models that previously gave 50 Ω suddenly gave impedance values that were off by about 4-6 Ω. While this difference seems small, in order to rectify this deficit in impedance, the dimensions of the trace or gap had to be altered by up to 30% of the original size. In the end, the successful CPW models in Sonnet had completely different dimensions from the CPW models in FEKO. The impedance graph for 1-20 GHz, shown in Figure 3.4, shows the impedance as centered closer to 55 Ω. To account for the thicker copper plating in Sonnet, I built the copper components as 3D objects on top of the substrate, and the resulting impedance, shown in Figure 3.5, was exactly 50 Ω at low frequencies, but very choppy at higher frequencies. This indicates that the design is now correct, though the high-frequency noise needs to be addressed.

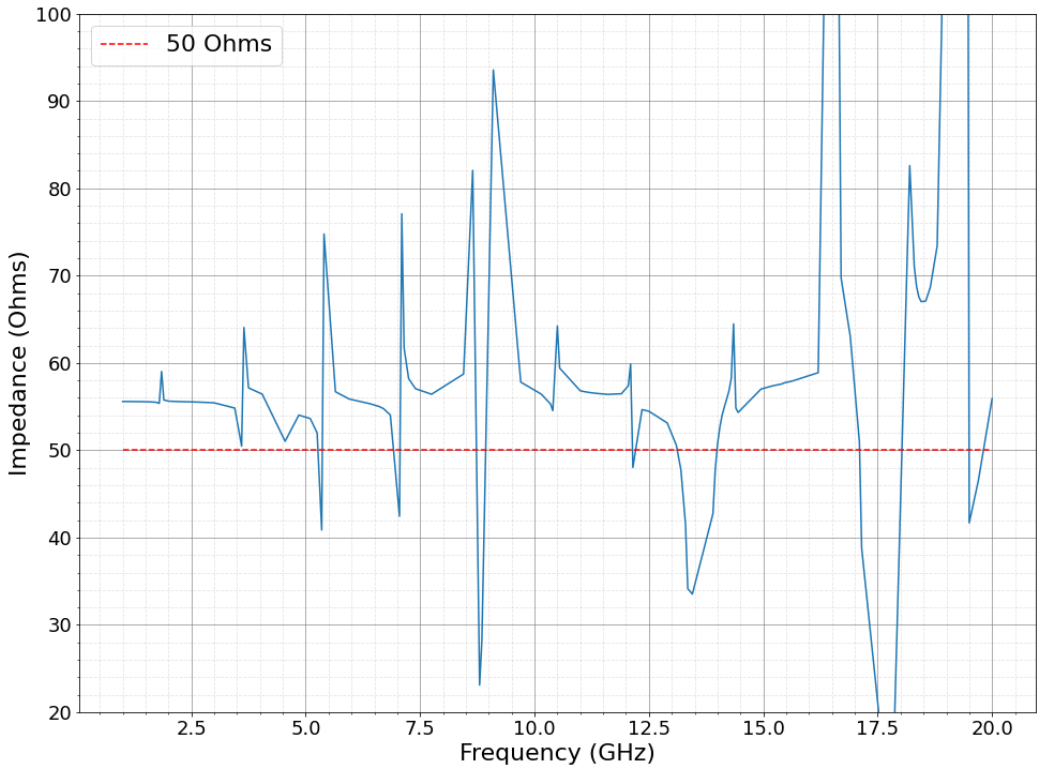

Figure 3.4: **2D Approximation: Impedance vs. Frequency**: This impedance plot shows the impedance behavior of a CPW originally configured for 50 Ω impedance, with a 2D plane approximation for the copper plating in Sonnet. The impedance is higher than expected across 1-20 GHz of frequency, centered at about 55 Ω.

After it was discovered that the thickness of the copper trace impacts the impedance of a CPW, the Sonnet simulations were modified to reflect a 3D trace rather than a planar approximation, as the additional dimension is used for CPW capacitance calculations and contributes to the impedance calculations.

3.2.2 High-Frequency Noise Reduction

Sonnet performs all calculations, notably impedance and resonance calculations, as though the model were sitting in a conducting box. If the microwaves were bouncing off the walls of this cavity, it might explain some of the interference and noise seen in Figures 3.4 and 3.5. Since the via fences had successfully reduced noise from microwaves

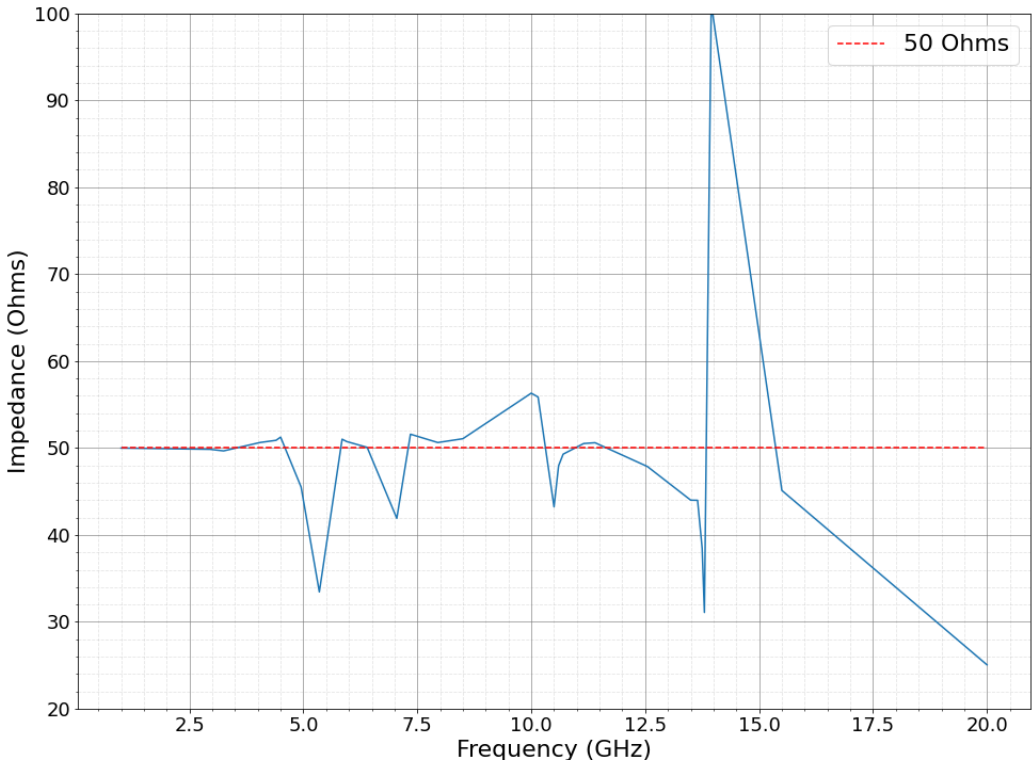

Figure 3.5: **3D Approximation: Impedance vs. Frequency:** This impedance plot shows the impedance behavior of a CPW originally configured for 50 Ω impedance, with a 3D object approximation for the copper plating in Sonnet. The impedance is as expected until about 4 GHz, where large peaks are introduced. This high-frequency noise is present all the way until 20 GHz.

jumping onto the upper groundplanes, a few vias were placed along the edges of the upper groundplanes in a short fence perpendicular to the center trace, as shown in Figure 3.6. This slight adjustment resulted in the impedance graph in Figure 3.7. Evidently, the edge vias successfully reduced impedance noise from environmental microwave reflections. Since the chip will be placed in an environment with other electronic components, these edge vias were introduced to the final prototype designs to isolate the center trace from the environment as much as possible.

After this modification was introduced to the CPW designs, the Sonnet simulations agreed with the calculations and with FEKO simulations, verifying the design for pro-

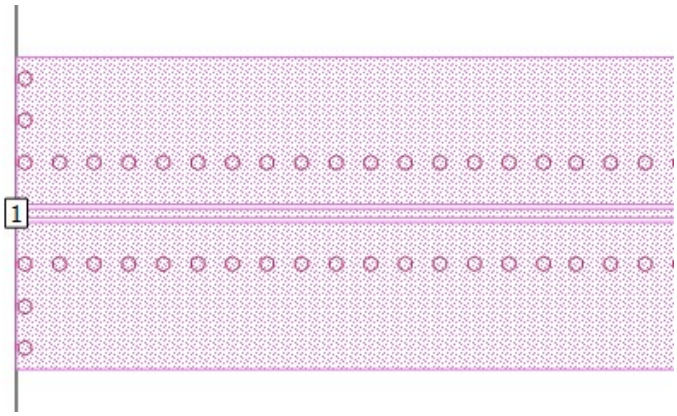

Figure 3.6: **Edge Vias Model** This Sonnet model shows the final CPW configured for 50 Ω impedance, with a 3D object approximation for the copper plating (pink) for the trace and upper groundplane and vias (circles) both parallel to the trace and along the edges of the CPW upper groundplanes. The boxed 1 indicates the microwave input port, and the lower groundplane is not shown.

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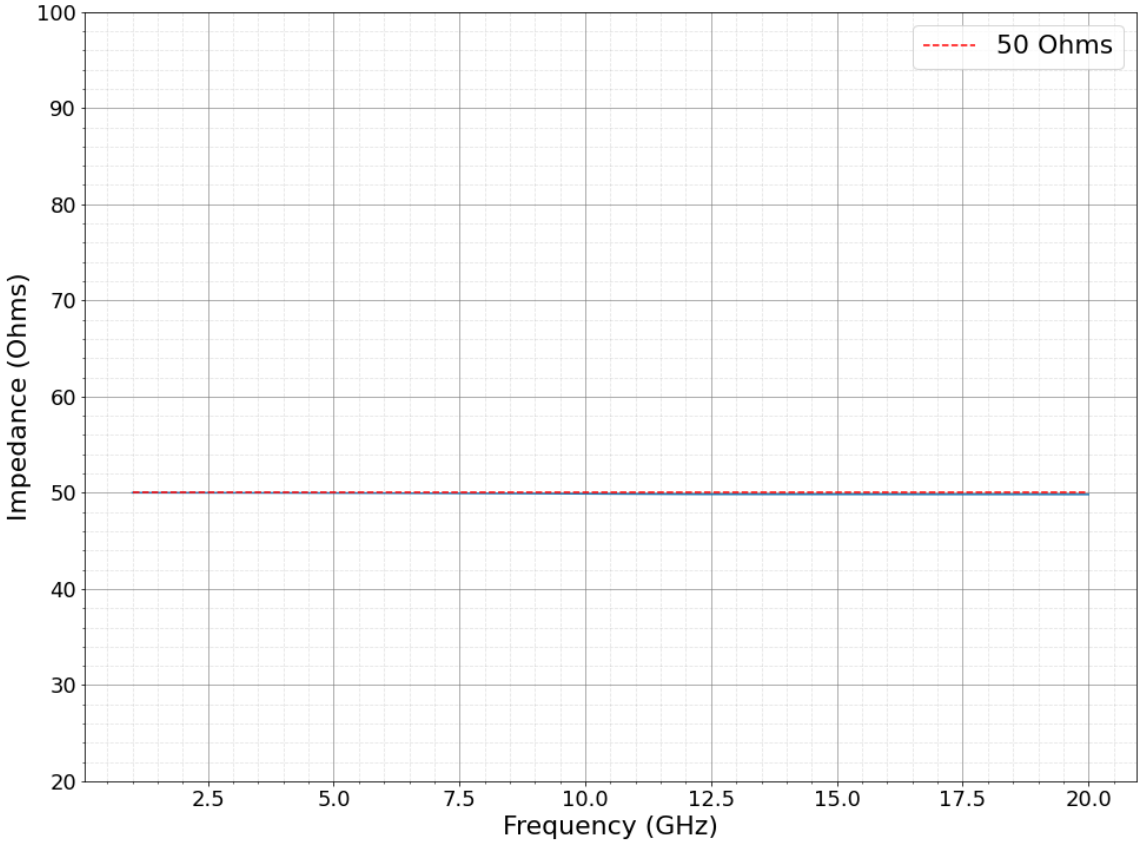

Figure 3.7: **Edge Vias: Impedance vs. Frequency:** This impedance plot shows the impedance behavior of a CPW originally configured for 50 Ω impedance, with a 3D object approximation for the copper plating and edge vias (Sonnet simulation). The impedance is almost exactly as expected across all 1-20 GHz, at 50$\pm$.2 Ω.

Chapter 4

Prototype Production and Preparation

In order to compare CPW design simulations with reality, four separate CPW transmission lines were constructed with varying dimensions. These prototype circuits can be used for testing impedance, CPW-to-connector coupling, and CPW-to-CPW coupling. A microstrip transmission line was also constructed to test CPW-to-microstrip coupling.

We ordered four unique CPW design from Cercuits BV (Geel, Belgium), with six samples of each design, for a total of 30 CPWs. Additionally, we ordered six samples of the microstrip design so that there are 36 prototype samples in total. The dimensions of the designs are given in Table 4.1.

All of the CPWs are non-tapered, and have different trace widths such that three of them can be used to construct a makeshift FCPW in the lab to test CPW-CPW coupling. The fourth CPW is a “microstrip CPW"– its center trace width is identical to the trace width on the microstrip, and is used for testing coupling between the CPW and the atom chip.

Additionally, these prototypes will be used for measuring the near field behavior for the microwave magnetic fields produced by the chips. Magnetic field strength will increase as trace size decreases, for a given frequency. The exact behavior will be simulated and verified using physical measurements of the magnetic fields along the CPW traces.

Prototype Dimensions				
Design Name	**Substrate Thickness (mm)**	**Trace Width (mm)**	**Gap Width (mm)**	**Copper Thickness (mm)**
CPW 1	1.00	1.08	2.15	0.035
CPW 2	1.00	0.60	0.35	0.035
CPW 3	1.00	0.20	0.11	0.035
CPW 4	1.00	0.20	0.11	0.035
CPW 5	1.00	0.38	0.199	0.035
Microstrip	0.038	0.38	-	0.035

Table 4.1: **Prototype Dimensions:** Each CPW and the microstrip are all designed to maintain 50 Ohm impedance. CPWs 1-4 are for testing the FCPW design and impedance along a series of connected samples. CPW 1 is the input (designed to match up with a coaxial cable), CPW 2 is the center of the FCPW, and CPWs 3 and 4 are for the CPW output and are designed at the smallest trace size producible by CERcuits. CPW 5 matches the trace width of the microstrip, and is designed to test CPW-microstrip coupling.

4.1 Prototype Quality Control

High levels of precision are required of the key CPW dimensions (gap width, trace width, substrate height, and copper thickness). For example, the calculated (expected) impedance value for the aforementioned CPW 5 is given as 50.04 Ω. A change in the gap width from 0.199 mm to 0.200 mm increases the impedance to 50.12 Ω. While this difference is ostensibly negligible, our simulations found that if a characteristic impedance is further than about $\pm 0.05\Omega$ from 50 Ω, the minute discrepancy causes resonant frequencies to bounce along the trace, increasing the reflection coefficient and decreasing overall reliability of the CPW.

Thus, all dimensions of the prototypes had to be carefully measured under a high-performance optical microscope called HIROX at William Mary's Applied Research Center (ARC) Core Labs (ISC3, room 1223). Measurements were typically made at $\times 35$ magnification. The HIROX microscope's measurement software allows a user to draw a line

on the magnified sample, and returns the length in μm. In order to ensure measurements were precise, and not based on a poorly-estimated perpendicular line, measurements were made using the program's angle feature to draw a 90° angle, which was then used as a reference for the lines drawn. The final product is shown in Figure 4.1, in which the trace and gap widths are measured along with a few via diameters. This measurement process was tedious but very rewarding: in addition to providing the average dimensions of the prototypes, inspections under the HIROX revealed defects and anomalies that would have severely impaired performance. A crack was found, for example, that completely split one trace, shown in Figure 4.2, that may cause noise in the impedance data if the microwaves are prevented from crossing this boundary. A full summary of the dimensions measured is provided in Appendix B.

The HIROX also illuminated some of the manufacturer's production methods. Figure 4.3 shows the serrated edge along the copper trace. Likely these small divots were produced by a pulsed-laser cutting method, indicating that the production method is highly accurate and unlikely to tear the copper or crack the AlN substrate. This increases confidence in the integrity of the sample. Figure 4.3 also shows, however, that the inner edge of the trace lacks these divots on either side, providing the fluctuation-free gap width that is crucial to maintaining constant impedance.

4.2 Connector Selection and Soldering

As discussed, these CPWs have been designed to carry microwaves from a coaxial cable to a microstrip. In testing, however, each CPW must be individually tested for performance before combining them all into an FCPW. Thus the original "input" CPW is not the only one that must be connected to a coaxial cable, and many coaxial connectors of varying sizes were acquired to ensure that each CPW could be effectively tested.

SMA connectors, a type of coaxial connector built for high-frequency electronics

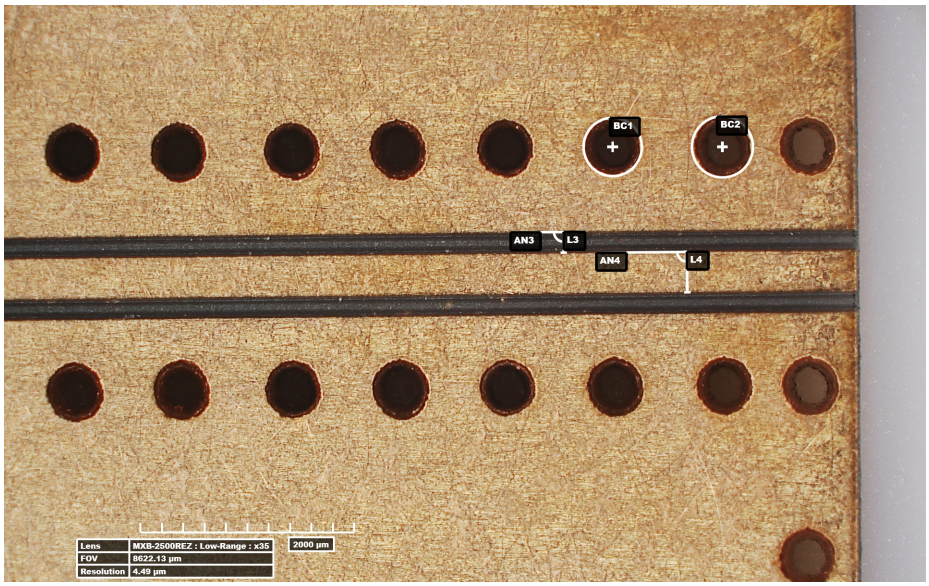

Figure 4.1: **CPW Measurement Process:** Measurements taken from APC's HIROX Optical Microscope at $\times 35$ magnification. Labels of AN refer to drawn angles of 90°, labels of L mark lines drawn against the side of an angle, and labels BC denote circles drawn to measure diameter of vias.

(typically rated for DC-18 GHz), were selected for the various CPW dimensions to be tested. The mechanics of soldering the connector were considered in these selections, as well as the electrical interfacing between the connector and the trace. The diagram in Figure 4.4 depicts the SMA connector components: the conductive center pin is soldered directly to the center trace, while the outer conducting sheath provides grounding, and the two are separated by a dielectric. Simulations by Cate Sturner found that a center pin slightly larger than the trace produced the most efficient coupling. The diameter of the dielectric also influences coupling, and best performance is achieved when the dielectric diameter matches the value of two or three trace widths.

Once chosen, the SMA connectors were soldered to the CPWs. Soldering to AlN proved unexpectedly challenging: its high thermal conductivity caused massive temperature fluctuations that hindered effective soldering. When cool, the substrate wicked away heat from the soldering iron so that the melted solder would not bond to the cop-

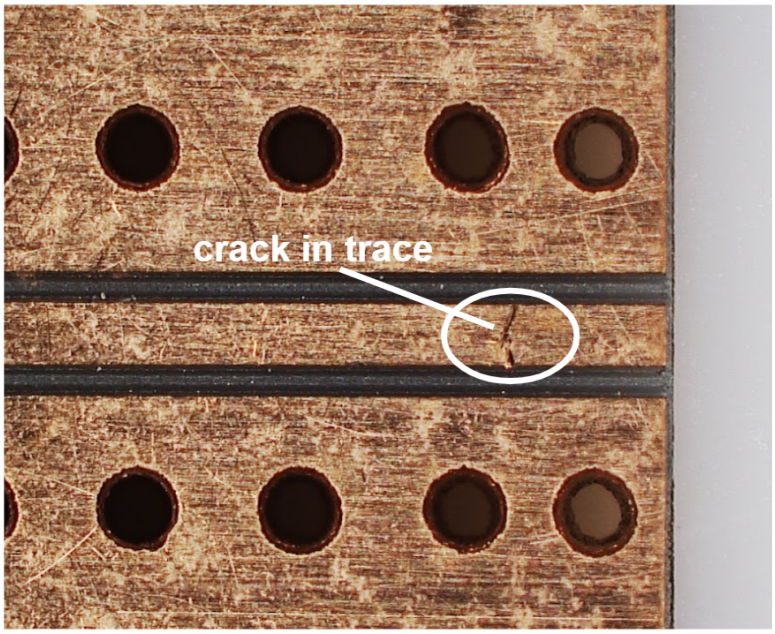

Figure 4.2: **Cracked Trace Defect** A crack (circled) in the copper trace splits the trace into two. Photo taken with the HIROX Optical Microscope at $\times 35$ magnification.

Figure 4.3: **Prototype Copper Edging:** Copper edging along the outside of the sample is serrated, while inner edges are smooth. Photo taken from APC's HIROX Optical Microscope at $\times 35$ magnification.

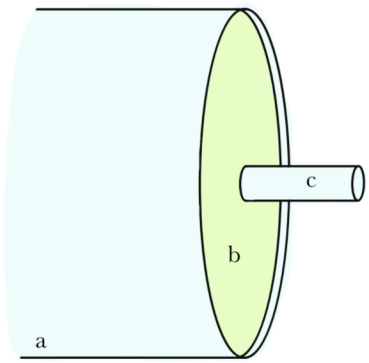

Figure 4.4: **SMA Connector Diagram:** Conductor components are depicted in cyan, and the dielectric (*b*) is shown in green. The center pin (*c*) connects directly to the center trace. Two outer pins (not shown) on the outer conductor (*a*) connect to the upper groundplanes, and two additional pins (not shown) connect to the lower groundplane.

per. To rectify this, soldering was moved to a hot plate to raise the temperature of the AlN. This is the only way that solder would bond to the copper. Unfortunately, once heated, the AlN held heat extremely well, even reaching reflow temperatures after significant contact with the soldering iron, and would melt previously-cooled solder. There is a small margin of time between these two states where soldering is easier– however, this did end up exacerbating the soldering process, as each connector pin had to be brought to about 100° C on the hot plate, soldered, and then removed from the hot plate onto a heat sink (a block of copper or aluminum), before being placed back onto the hot plate to solder the next pin.

The physical limitations of a soldering iron also needed to be considered. For CPW 1 (the largest), soldering by hand was precise enough to solder the small SMA pins to the copper components on the CPW. The others, however, require a much more precise soldering method. As the gap width decreases, there's also the added danger of bridging, so the soldering method needed to be precise and easily controlled.

One method explored was a combination of hand-soldering and the use of solder paste. Typically, solder paste is handled in a reflow oven or with a hot air gun, but hand soldering ensured that bridging could be addressed immediately, without having to bring the solder back up to reflow temperatures. The limitation of this approach is the size of the soldering iron: even the smallest iron tips were much larger than the solder paste syringe, making it difficult to bring the solder to reflow temperatures on the smallest CPWs even if it could be applied with the syringe. Melting the solderpaste with a soldering iron also fails to fully melt all of the solder balls. Magnified 35 times under the HIROX Optical Microscope, these imperfections are clearly shown in Figure 4.6: there are solder balls on the outskirts of the melted solder, and all of the solder is encased in flux residue, indicating that it was not evenly and thoroughly heated to reflow temperatures in this method. In contrast, Figure 4.5 shows a similar photo from the HIROX of a model soldered by hand with traditional solder. This solder is even and lacks the abundance of flux residue present in Figure 4.6.

The final method still uses solderpaste, but takes advantage of the WM Makerspace reflow oven. This method is expected to more thoroughly heat the solder, eliminating loose solder balls. One potential disadvantage is that the temperature must be preprogrammed as a full thermal profile, and doesn't allow for the heat-and-cool sequences that have facilitated hand soldering for the AlN substrate.

4.3 Microwave Insertion Efficacy Tests

High-frequency waves, like the microwaves used in the atom interferometer, prove difficult to control in electronics. In previous CPW tests, Sindu Shanmugadas and I found that microwaves easily jump from one trace to another, and I encountered similar problems with my FCPW models before introducing vias. In simulation, many of these were able to be avoided with the addition of groundplanes, vias, increased gap width between

Figure 4.5: **Handsoldering Method**: The solder is even and thick, with visible flux residue on the gap, but little or no flux residue on the solder itself. Photo taken under the HIROX Optical Microscope at ARC Core Labs at $\times 35$ magnification.

the upper groundplanes and trace, etc., but all of these solutions required high levels of precision.

4.4 Microstrip CPW to Microstrip Interface

A central focus of the prototype testing was to investigate the interfacing between the microstrip CPW and the microstrip. Since the two components have different substrate thicknesses (1.0 mm for microstrip CPW and 0.38 mm for the microstrip) it was essential to ensure a strong connection between the two, both mechanically and electrically.

The microstrip prototype, shown in Figure 4.7 is thinner to reflect designs of the atom chip, and all the CPWs were the same thickness so that the FCPW design could be produced on one substrate. The height of the substrate changes the impedance along the trace, and 1.0 mm was the optimal thickness to maintain 50 Ohm impedance for the range of trace widths necessary to connect between the coaxial cable and the microstrip.

Figure 4.6: **Solderpaste with Soldering Iron Method**: The solder is covered in visible flux residue, and there are solder balls that never reached reflow temperatures all around the fully melted solder that is directly on the connector. Photo taken under the HIROX Optical Microscope at ARC Core Labs at $\times 35$ magnification.

Thus the microstrip CPW samples are a different thickness than the microstrip samples, and connecting them required a new method to level them out. The results of these tests are discussed in Section 5.2.

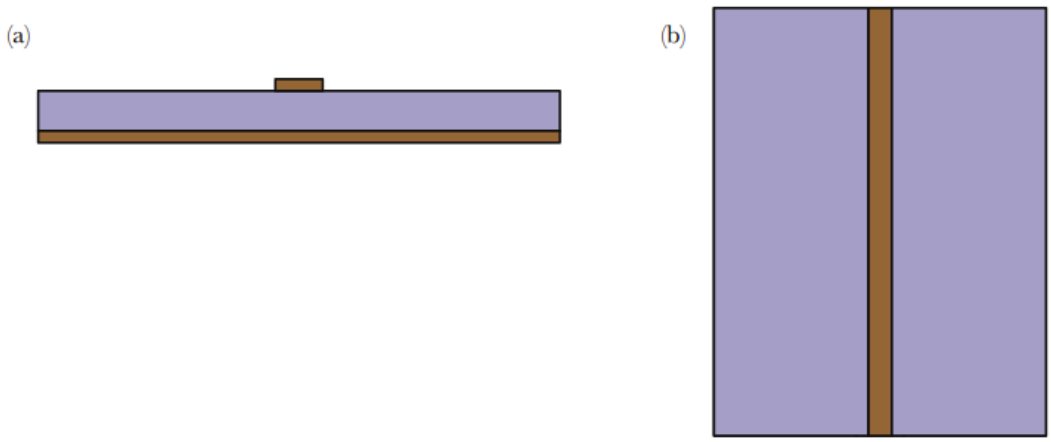

Figure 4.7: **Microstrip Transmission Line Geometry**: In figures (a) and (b), components of thin copper plating are brown and aluminum nitride (AlN) substrates are lilac. Dimensions not to scale. (a) Side view of the microstrip, consisting of a single copper trace on an AlN substrate atop a copper groundplane. The ratio of the width (0.38 mm) to the height (0.38 mm) yield 50 Ohm impedance. (b) Top view of the microstrip, with a straight center trace on the lilac AlN substrate, grounded by a copper groundplane (not visible).

Chapter 5

Prototype Performance

This chapter presents the main results of testing the impedance for the CPW and microstrip prototypes using a vector network analyzer (VNA). Section 5.1 presents tests on individual CPW prototypes, and Section 5.2 describes the performance of the CPW-to-microstrip connection. Finally, Section 5.3 presents the results of CPW-to-CPW coupling, to make the FCPW using multiple CPW prototypes as FCPW segments.

The main concern in analyzing performance data is the presence of resonance peaks in the impedance data, since they're caused by some resonance cavity that's likely in the chips themselves. Resonances caused by a cavity are periodic in nature, and measurable on the impedance plots collected for these tests. The distance between resonance peaks, the free spectral range, is given by

$$\Delta f_{fsr} = \frac{c}{2L}, \tag{5.1}$$

where Δf_{fsr} is the free spectral range, c is the speed of light in the medium, and L is the length of the cavity producing the peaks. The speed of light in AlN is given by the relationship

$$c = \frac{c_{vacuum}}{n} \tag{5.2}$$

where n is the index of refraction and c_{vacuum} is the speed of light in a vacuum.

n is easily calculated as the square root of a known constant (the effective dielectric constant, about 4.7 for our models) and found to be 2.168. The speed of light in the AlN medium is 1.3889×10^8 m/s. Thus by calculating the average distance between impedance peaks by measuring them on the impedance plots, an estimate can be made for the length of the cavity. All the samples are 3.0 cm long and 2.0 cm wide. With connectors attached to a single CPW and an SMA barrel on one side (this was the standard setup for all tests performed), the length is 6.6 cm; attaching connectors and an SMA barrel to a single-step FCPW (with two CPWs) brings the length to 9.65 cm. Comparing the cavity length to the length of the setup can be used to identify what design feature is producing a cavity in noisy CPWs and microstrips.

5.1 Individual CPWs

Before piecing CPWs into the combined FCPW, a few samples from each set of dimensions were selected, soldered, and tested for impedance performance. Samples were labeled A-F for testing purposes, to match them with their measured dimensions from quality control. SMA connectors were soldered onto either end of the CPW to be tested, and connected to the Vector Network Analyzer (VNA) coaxial cables. The VNA then measured the characteristic impedance based on a wide range of frequencies, typically ranging from 1 GHz to 20 GHz.

CPW 1 Samples A and F were each tested with SMA connectors of different sizes. Both successfully transmitted microwaves but also had significant resonances. Their impedance plots are shown in Figures 5.2 and 5.1, respectively. The noise is possibly due to the amount of solder, as this could increase the impedance or cause a resonant cavity to form, or lead to small gaps left between the connector and substrate, which may hinder the effective transfer of microwaves. These gaps were eliminated in future tests by taping connectors down before soldering.

Sample 1F was tested first with a larger SMA connector. As shown by Figure 5.1, the impedance has significant resonances; while it does center around 50 Ω at low frequencies, this stability only last until about 5 GHz, and the highest peaks are well over 500 Ω. The measured Δf_{fsr} is 1.2 GHz, which corresponds to a calculated cavity length of 5.79 cm: on the model with connectors attached this corresponds to nearly the full length of the chip-and-connectors system, ending in the middle of the output connector.

Sample 1A was tested next, with a new SMA connector that featured a smaller center pin and larger grounding pins. The amount of solder used was reduced in attempt to alleviate some of the resonances. Figure 5.2 depicts the improvements in the impedance: overall, the resonance structures are smaller, with the highest peak just exceeding 175 Ω, and the impedance is centered around 50 Ω until about 7 GHz. The Δf_{fsr} for this test is 1.4 GHz, for a cavity length of 4.96 cm, the precise distance from one connector to the start of the SMA barrel on the other side.

5.2 Microstrip-CPW Coupling

Like the CPWs, a few select microstrip models were tested individually before being soldered to the microstrip CPW to test coupling between the two interfaces. Soldering the microstrip models raises a unique challenge, however: in addition to having the same tricky thermal properties at the CPWs, they are less than half as thick.

In the first test, microstrip Sample A was hand-soldered to an SMA connector and connected directly to the VNA for testing. Unfortunately, the large VNA coaxial cables were too heavy for the fragile sample and snapped it in half before data could be collected.

In the second test, microstrip Sample B was similarly prepared and connected to the VNA with a smaller, more flexible coaxial cable on either side to alleviate some of the tension. The resulting data was extremely noisy, as shown in Figure 5.3, with low-frequency

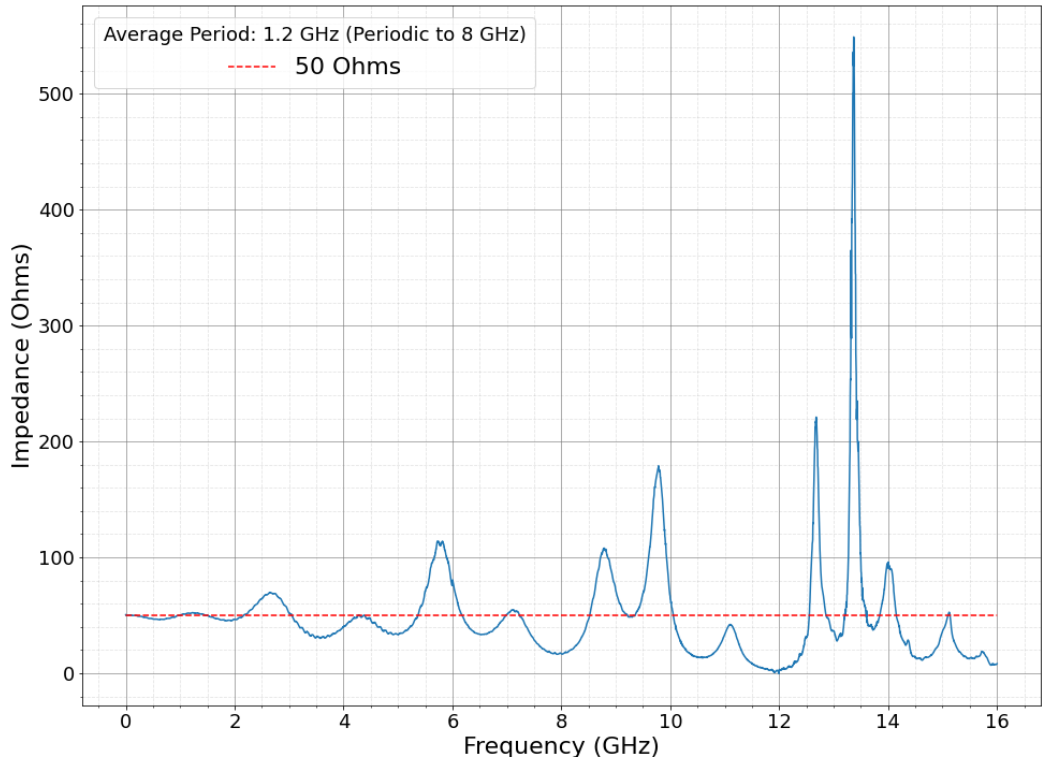

Figure 5.1: **CPW 1, Sample F: Impedance vs. Frequency**: This plot shows the characteristic impedance of CPW 1 (Sample F) centers around 50 Ω (depicted as a red dotted line) until it reaches around 5 GHz. The noise peaks, though they vary in height, are equally spaced until 8 GHz, with an average separation distance of 1.2 GHz. This average separation is the free spectral range.

spiked reaching over 3500 Ω, and consistent spikes up through 20 GHz. The distance between the impedance peaks is constant until around 8 GHz, so the average period was calculated and found to be 1.2 GHz. The Δf_{fsr} is shorter than the other models, at 0.579 GHz, and corresponds to a longer cavity length of 11.99 cm. This model was attached to short cables (about 15 cm each) on either side, so it makes sense that it might have a longer cavity length. While the additional cables should not have drastically reduced performance, the delicacy required to attach them may have reduced the security of the connections. This possibility required that the microstrip sample be tested without the cables to ensure the problem was not with the sample itself, so graduate student

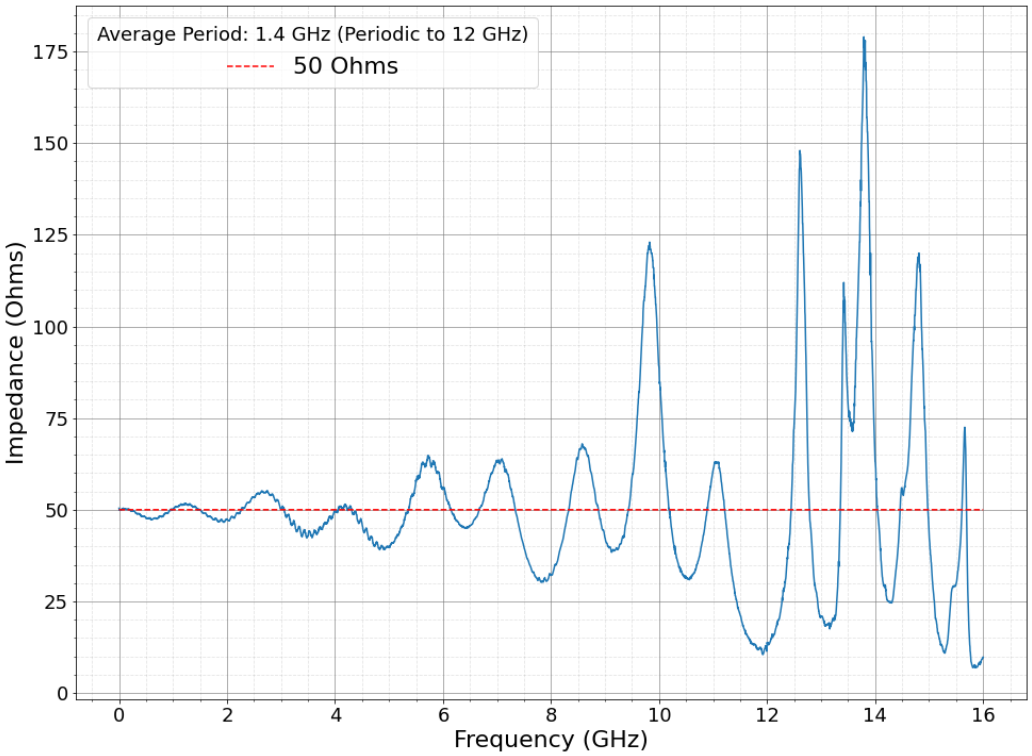

Figure 5.2: **CPW 1, Sample A: Impedance vs. Frequency**: This plot shows the characteristic impedance of CPW 1 (Sample A) centers around 50 Ω (depicted as a red dotted line) until it reaches around 7 GHz. The noise peaks, though they vary in height, are equally spaced until 12 GHz, with an average separation distance of 1.4 GHz. This average separation is the free spectral range.

William Miyahira offered to counter the pressure of the coaxial cable as it was screwed onto the connector. This method successfully avoided breaking the sample, and Figure 5.4 shows the improvement in the impedance. While still noisy, the impedance after an initial spike is much closer to 50 Ω. Without the cords attached, the Δf_{fsr} is 1.51 GHz and the cavity length is 4.61 cm. Again, this corresponds very closely to the distance from one connector to the SMA barrel on the opposite end of the chip.

In the third test, a piece of sheet metal was cut to fit against the microstrip and around the soldered connectors, then glued to the lower groundplane. This backing provided extra reinforcement for the chip, and allowed for the VNA cables to attach much

more securely since it could withstand a tighter fit in the cables. As shown in Figure 5.5, the performance drastically improved: Unlike the previous two trials, there is a region of good performance, until about 5 GHz, and the noise peaks reach 250 Ω rather than the prior peaks of ten times this size. Unfortunately, the chip did break unexpectedly during data collection, where the backing ended so as to leave room for a connector.

To prevent this breaking from occurring again, a higher-coverage backing was prepared with small cutouts for the connectors that allowed the sheet metal backing to reach all four corners of the microstrip chip. As shown in Figure 5.6, the low-frequency behavior is relatively stable until about 3 GHz, and while the higher frequencies do have higher noise peaks, this plot shows more smoothness in the data (compared with Figure 5.5) that indicates that the backing successfully stabilized the microstrip.

5.3 FCPW

The first FCPW was a simple one-step taper between CPW 1, the largest CPW, and CPW 2, the next size down. The two CPWs were aligned, soldered along the entire joint on the bottom, and then a thin copper wire was hammered flat (to emulate a copper ribbon, as opposed to a round wire) and soldered across the joint to the traces on either side. When attached to the VNA, the weight of the cables bent the FCPW at the joint, possibly breaking the ribbon. While the FCPW was removed from the wires and resoldered to secure the connection and reinforce the bottom, this break may have caused the excessive noise seen in Figure 5.7. The Δf_{fsr} is 0.814 GHz, and the cavity length is found to be 8.53 cm. This is nearly the full length of the test setup, ending near the end of the SMA barrel or at the end of the connector.

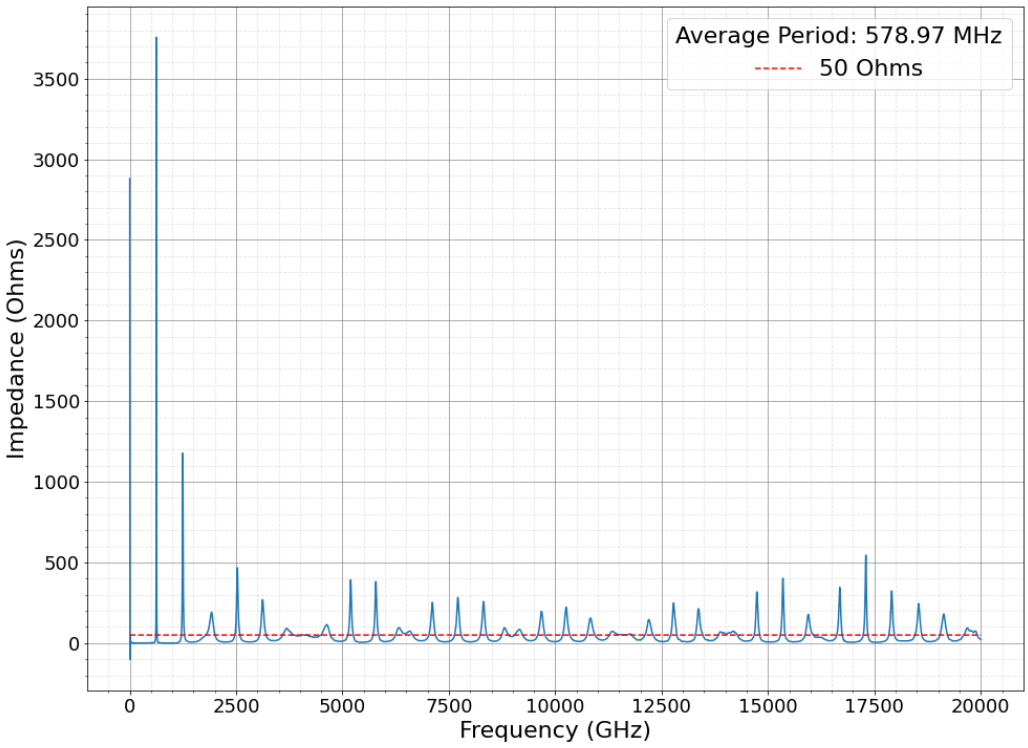

Figure 5.3: **Microstrip Sample B, with attachments**: This plot shows the measured impedance of microstrip Sample B, which had a small coaxial cable on either side. The impedance is noisy across all frequencies, reaching over 3500 Ω and never really centers around 50 Ω (red dotted line). The noise peaks are equally spaced for the full range of 20 GHz, with an average separation distance of 0.579 GHz (578.97 MHz). This average separation is the free spectral range.

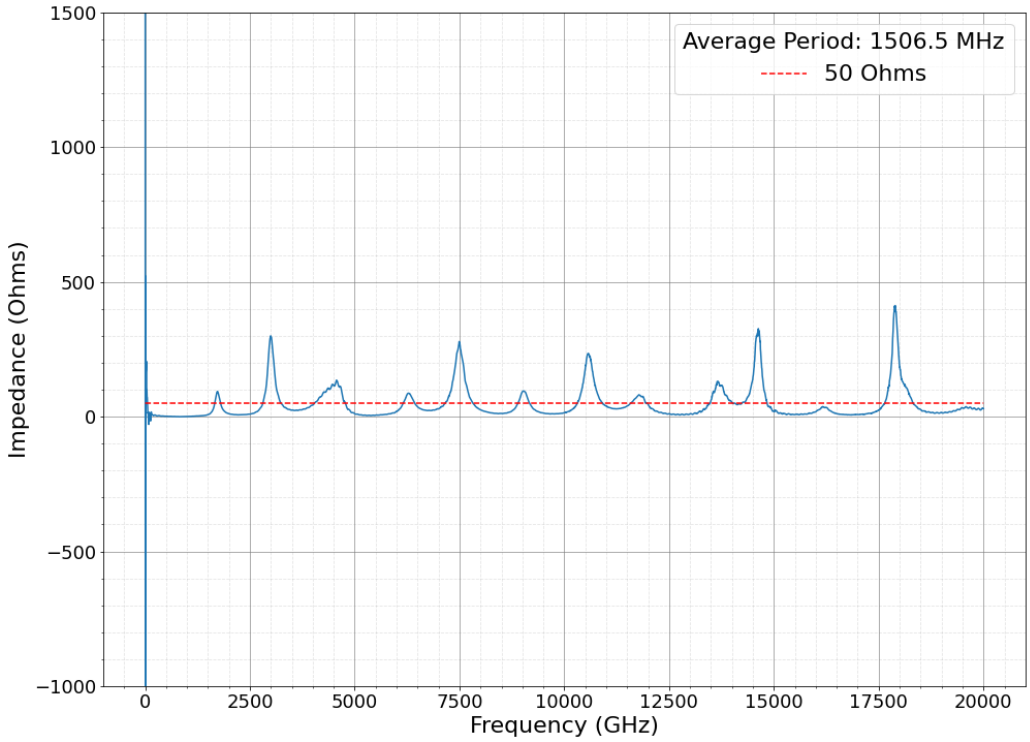

Figure 5.4: **Microstrip Sample B, without attachments**: This plot shows the measured impedance of microstrip Sample B connected directly to the Vector Network Analyzer cables. The impedance is noisy across all frequencies, rising to well over 2000 Ω at 0 GHz and never really centers around 50 Ω (red dotted line). After the first spike, there are periodic sequences of two-three spikes that are predictably spaced apart. The highest peaks in these clusters are nearly equally spaced for the full range of 20 GHz, with an average separation distance of 1.507 GHz (1506.5 MHz). This average separation is the free spectral range.

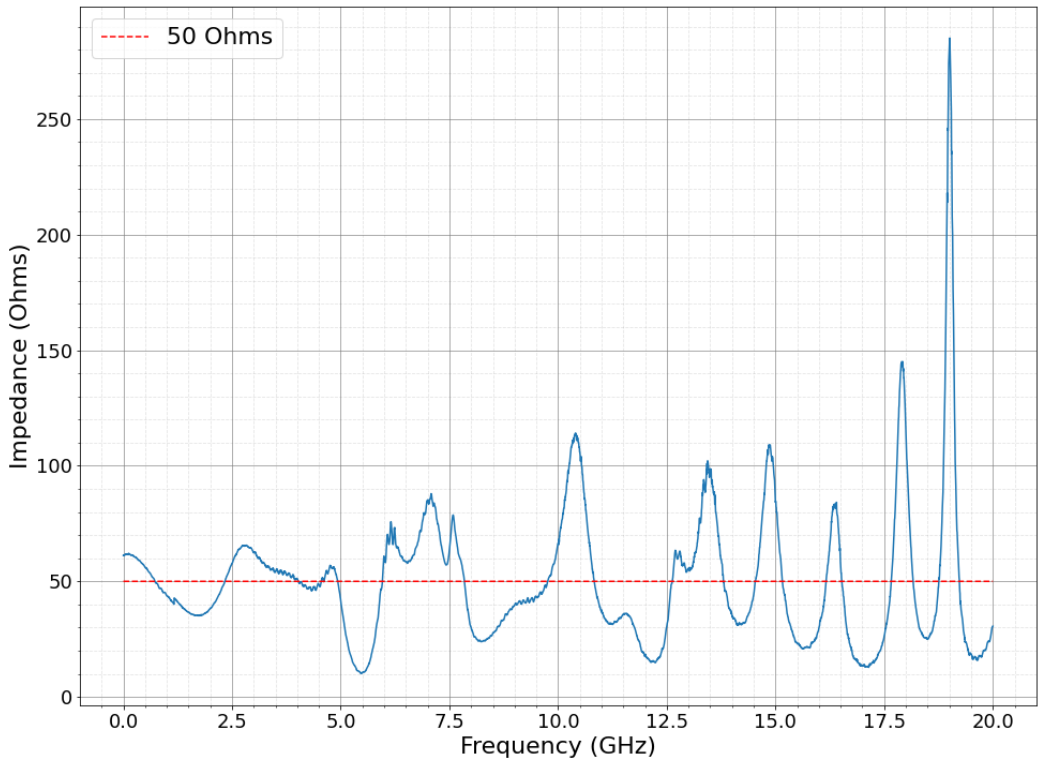

Figure 5.5: **Microstrip Sample D, with backing**: This plot shows the measured impedance of microstrip Sample D, which had a piece of sheet metal affixed to the bottom groundplane. The impedance is noisy at frequencies above 5 GHz, reaching just above 250 Ω at the highest peak. Overall, the performance is good at low frequencies and very noisy above 5 GHz. The resonance peaks do not exhibit strong periodic behavior.

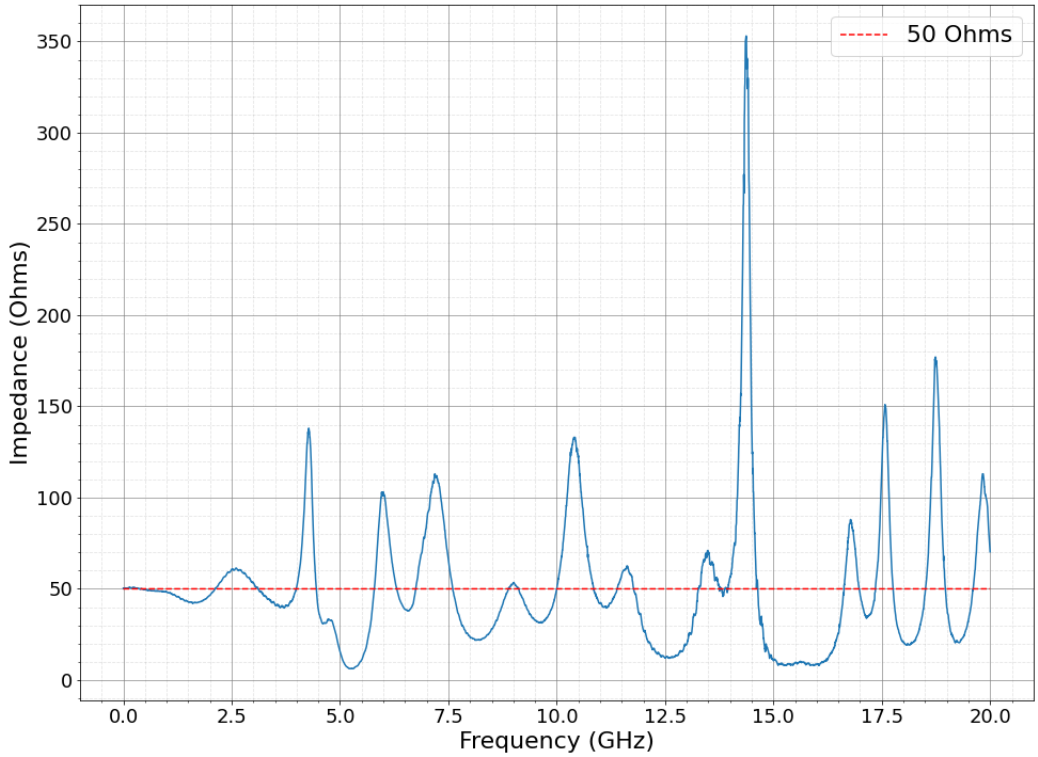

Figure 5.6: **Microstrip Sample E, with backing**: This plot shows the measured impedance of microstrip Sample E, which had a high-coverage backing and very small cutouts for the connectors and solder. The impedance is noisy across frequencies above about 3 GHz, reaching over 350 Ω at the highest peak. The low-frequency behavior is relatively stable.

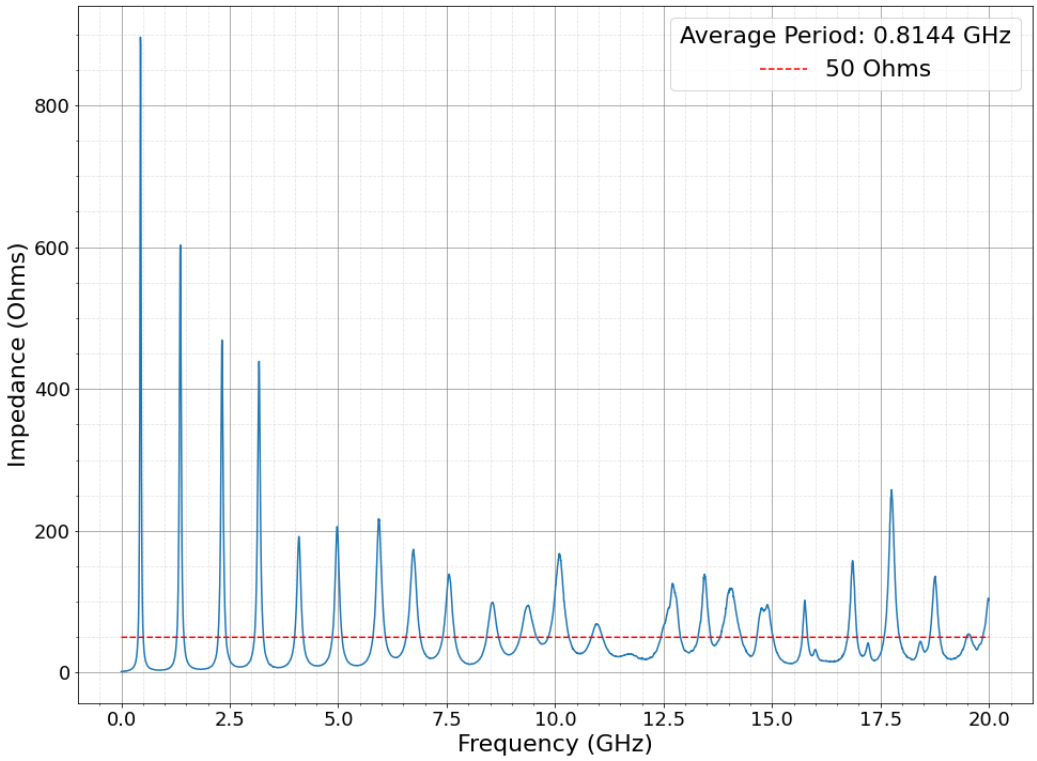

Figure 5.7: **One Step FCPW**: This plot shows the measured impedance of a one-step FCPW, from CPW 1 to CPW 2, connected directly to the Vector Network Analyzer cables. The impedance is noisy across all measured frequencies, rising over 800 Ω at its highest peaks, and never centers around 50 Ω (red dotted line). The resonance peaks are highly periodic, with an average separation of 0.8144 GHz across all 20 GHz of frequency. This average separation is the free spectral range.

Chapter 6

Conclusion

This project demonstrated successful microwave transmission through a CPW and microstrip. Most successful were the straight CPW tests with large CPWs, which showed stable microwave transmission until about 5 GHz. Tests of microwave transmission in a microstrip were similarly successful at low frequencies, where impedance was stable under 3-5 GHz. Initial FCPW tests were highly noisy and did not give a stable region even at low frequencies.

Most of the resonance peaks in impedance plots were regularly spaced, indicating a cavity is present that is generating the resonances. The spacing of the peaks did not correlate to a distance along the chips, but extended into the connectors and SMA barrel attached to the samples themselves. Initial comparisons of the cavity lengths to the samples, as set up for testing, did not reveal any obvious source of a cavity. However, the cavity lengths did correspond to the actual test setups: the cavity length was about twice as long for the one-step FCPW as for the regular CPW and microstrip samples, and the cavity length for the microstrip test with additional cords attached was significantly longer than any of the previous tests.

These peaks might be due to loose attachments, especially since the noise was worse on the microstrip models, whose fragility makes them difficult to tightly screw into the VNA cables. It may also be that the SMA barrels are damaged or old, though they would

all have to be damaged since a number of barrels were used for testing, or that there is simply poor coupling between the test setup pieces (sample, connectors, and SMA barrel) and the VNA cables. Another strong possibility is that the dielectric constant of the manufactured AlN substrate is not the precise value we designed for. If the dielectric constant is inaccurate, this could offset the impedance from 50 Ω and cause resonances due to poor impedance matching between the chip and the rest of the system. It is worth noting, however, that some of the samples did show regions of stability around 50 Ω, and if the dielectric constant were inaccurate we would expect to see an offset. This could be verified by running simulations of CPWs with the prototype dimensions and with variations in the dielectric constant. The dielectric constant could also be calculated with the prototypes, by estimating a cavity length and solving for the effective dielectric constant. Overall, further investigation is required to determine the source of these cavities and identify a strategy for eliminating them.

In the context of spin-squeezing in an FCPW, further experimental work is needed to determine if the magnetic field strength increases as the CPW narrows. While early simulation did demonstrate an increase in field strength, this has not yet been investigated in a prototype.

Overall, the biggest contribution of this project was to prepare the way for further work in CPWs and FCPW prototyping. Full documentation, including photographs taken under the HIROX Optical Microscope and detailed measurements, was compiled for this first prototype order. The soldering process for connectors and for FCPWs was also characterized for future work. Initial tests were completed, and measurements taken, for the investigations into CPW effectiveness, microstrip-CPW coupling, and FCPW transmission. All work completed significantly advances the effort toward the goal to provide successful microwave insertion into the atom chip and increase interferometric precision through spin-squeezing.

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Appendix A

Python Plots

This simple function facilitates easily converting data from the Vector Network Analyzer imported as a *.csv* file to a Python plot.

```
import pandas as pd
import numpy as np
import matplotlib.pyplot as plt


def make_plots(data, save_as, size=4001):
  freq = data['TR1.FREQ.GHZ'].values
  imped = data['TR1.REAL IMPEDANCE.ohm'].values
  red = [50]*size


  plt.plot(freq, imped)
  plt.rcParams["figure.figsize"] = (16,12)
  plt.plot(freq, red, '--',color='r', label='50 Ohms')
  plt.legend(fontsize=22)


  plt.ylabel('Impedance (Ohms)', fontsize=22)
  plt.yticks(fontsize=18)
```

```
plt.xticks(fontsize=18)
plt.xlabel('Frequency (GHz)',fontsize=22)
plt.grid(b=True,which='major', color ='grey', linestyle='-', alpha=0.8)
plt.grid(b=True,which='minor', color ='grey', linestyle='--', alpha=0.2)
plt.minorticks_on()
plt.savefig('/content/drive/MyDrive/Research/'+str(save_as))‘
```

Appendix B

CPW Dimension Measurements

Select CPWs were chosen and carefully measured under the HIROX Optical Microscope. The trace width and gap widths were each measured twice, once on each end of the trace. The percent difference was calculated for the trace widths by comparing the average of the two with the nominal measurement. Two vias were measured for diameter and circumference, and general smoothness of edges. Overall inspection was completed on each one, even if it was not measured, to look for defects such as cracks, breakage along the edges, or debris. These measurements are accurate to the first two decimal places, with uncertainty of about ± 0.005 mm.

Prototype Nominal Dimensions				
Design Name	**Substrate Thickness (mm)**	**Trace Width (mm)**	**Gap Width (mm)**	**Copper Thickness (mm)**
CPW 1	1.00	1.08	2.15	0.035
CPW 2	1.00	0.60	0.35	0.035
CPW 3	1.00	0.20	0.11	0.035
CPW 4	1.00	0.20	0.11	0.035
Microstrip CPW	1.00	0.38	0.199	0.035
Microstrip	0.038	0.38	-	0.035

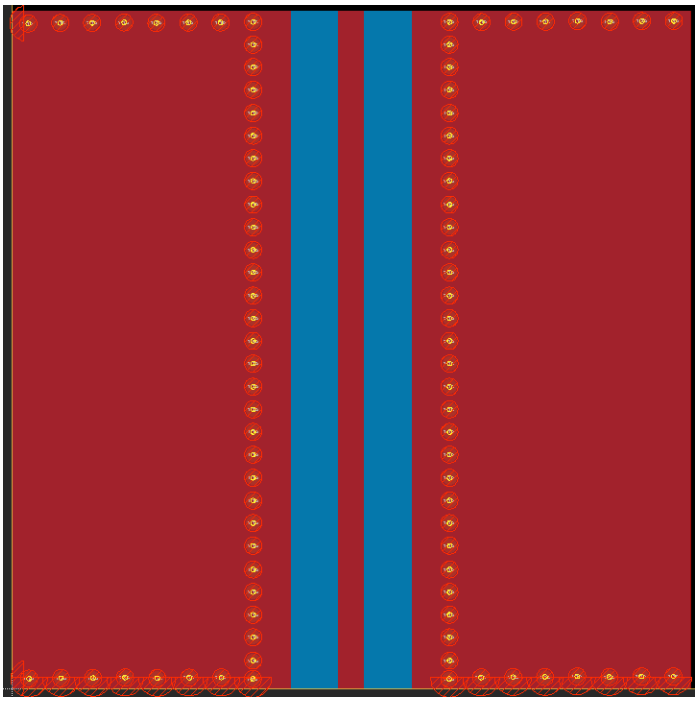

Figure B.1: **CPW 1 Schematic**: Depicted is a schematic in Fusion's EAGLE CAD program for designing electronics. The dimensions of gap width and trace width are for the input CPW 1, designed with 0.035 mm copper thickness. The AlN substrate is shown in blue, with the copper trace and upper groundplanes in red. Yellow vias (with red outline) are shown along three edges of the upper groundplanes, and connect through the substrate to the lower groundplane (not shown).

Prototype Measured Dimensions: CPW 1					
Sample	**Trace Width 1 (mm)**	**Trace Width 2 (mm)**	**Gap Width 1 (mm)**	**Gap Width 2 (mm)**	**Trace Percent Difference**
A	1.07	1.068	2.156	2.151	1.02%
B	1.054	1.075	2.151	2.137	1.44%
C	1.079	1.084	2.138	2.134	0.14%
D	1.088	1.084	2.127	2.126	0.56%
E	1.090	1.084	2.128	2.131	0.65%
F	1.103	1.103	2.134	2.138	2.13%

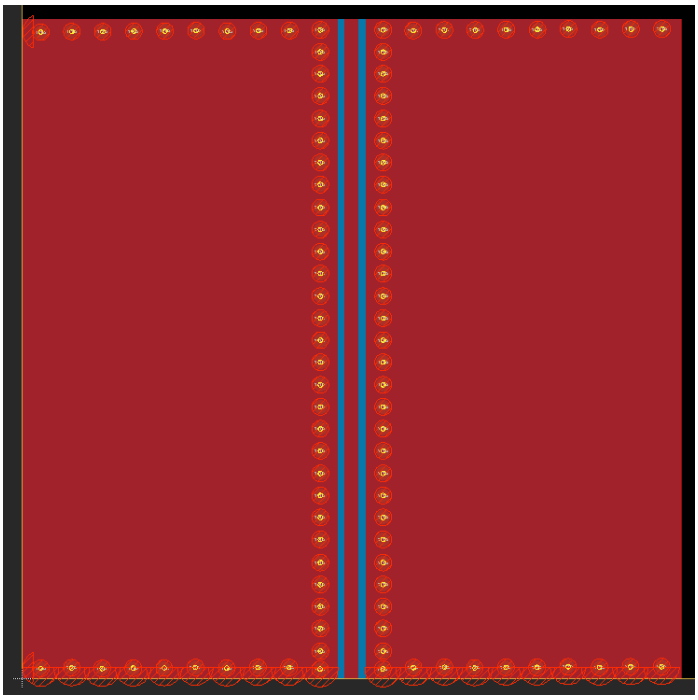

Figure B.2: **CPW 2 Schematic**: Depicted is a schematic in Fusion's EAGLE CAD program for designing electronics. The dimensions of gap width and trace width are for the transitional CPW 2, designed with 0.035 mm copper thickness. The AlN substrate is shown in blue, with the copper trace and upper groundplanes in red. Yellow vias (with red outline) are shown along three edges of the upper groundplanes, and connect through the substrate to the lower groundplane (not shown).

Prototype Measured Dimensions: CPW 2					
Sample	**Trace Width 1 (mm)**	**Trace Width 2 (mm)**	**Gap Width 1 (mm)**	**Gap Width 2 (mm)**	**Trace Percent Difference**
A	0.598	0.592	0.364	0.363	0.82 %
B	0.606	0.606	0.346	0.346	1.04 %
C	0.603	0.597	0.355	0.347	0.03 %
D	0.595	0.610	0.356	0.344	0.42 %
E	-	-	-	-	- %
F	0.592	0.602	0.363	0.365	0.50 %

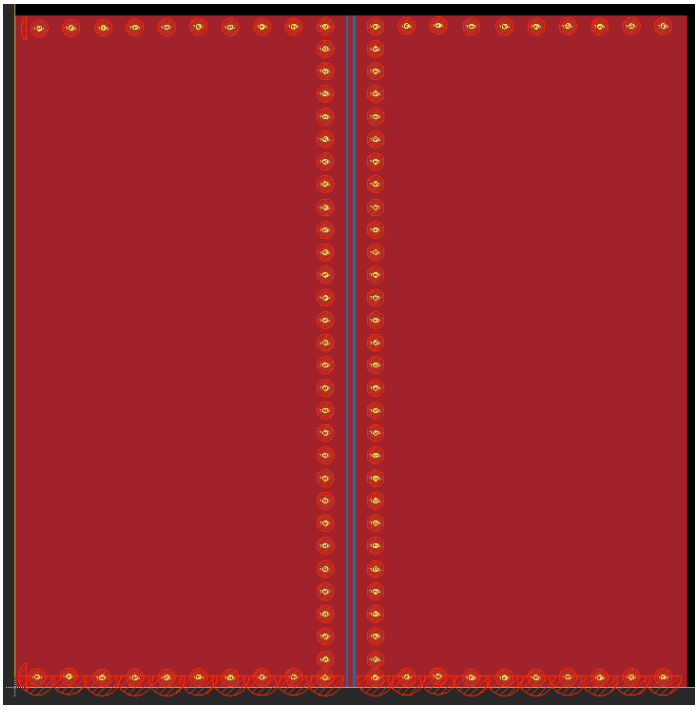

Figure B.3: **CPWs 3 and 4 Schematic**: Depicted is a schematic in Fusion's EAGLE CAD program for designing electronics. The dimensions of gap width and trace width are for the output CPWs 3 and 4, designed with 0.035 mm copper thickness. The AlN substrate is shown in blue, with the copper trace and upper groundplanes in red. Yellow vias (with red outline) are shown along three edges of the upper groundplanes, and connect through the substrate to the lower groundplane (not shown).

Prototype Measured Dimensions: CPW 3					
Sample	**Trace Width 1 (mm)**	**Trace Width 2 (mm)**	**Gap Width 1 (mm)**	**Gap Width 2 (mm)**	**Trace Percent Difference**
A	0.211	0.204	0.092	0.108	3.65 %
B	0.196	0.203	0.115	0.107	0.23 %
C	0.207	0.195	0.103	0.110	0.62 %
D	0.206	0.204	0.101	0.103	2.50 %
E	-	-	-	-	- %
F	-	-	-	-	- %

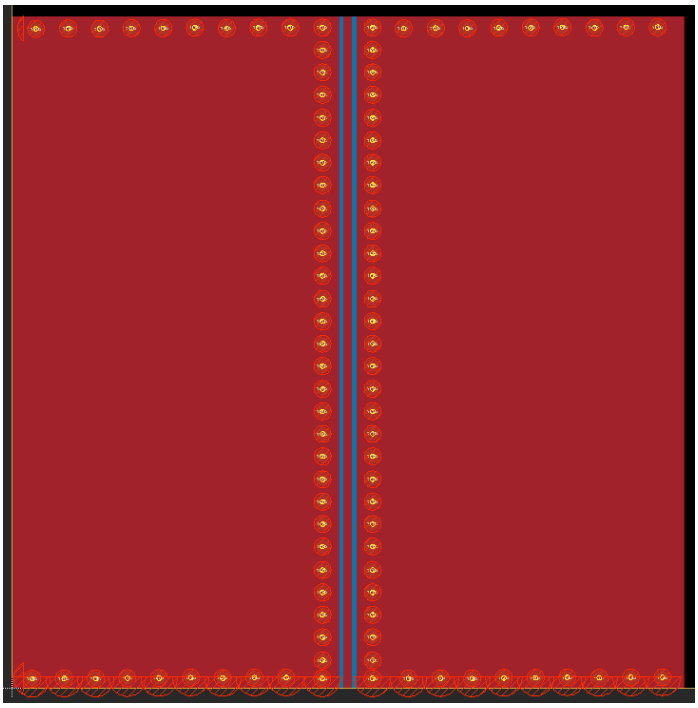

Figure B.4: **Microstrip CPW Schematic**: Depicted is a schematic in Fusion's EAGLE CAD program for designing electronics. The dimensions of gap width and trace width are for the microstrip CPW, designed with 0.035 mm copper thickness. The AlN substrate is shown in blue, with the copper trace and upper groundplanes in red. Yellow vias (with red outline) are shown along three edges of the upper groundplanes, and connect through the substrate to the lower groundplane (not shown).

Prototype Measured Dimensions: CPW 4					
Sample	**Trace Width 1 (mm)**	**Trace Width 2 (mm)**	**Gap Width 1 (mm)**	**Gap Width 2 (mm)**	**Trace Percent Difference**
A	0.208	0.218	0.095	0.089	6.50 %
B	0.203	0.227	0.102	0.086	7.50 %
C	0.201	0.202	0.102	0.102	0.80 %
D	-	-	-	-	- %
E	-	-	-	-	- %
F	-	-	-	-	- %

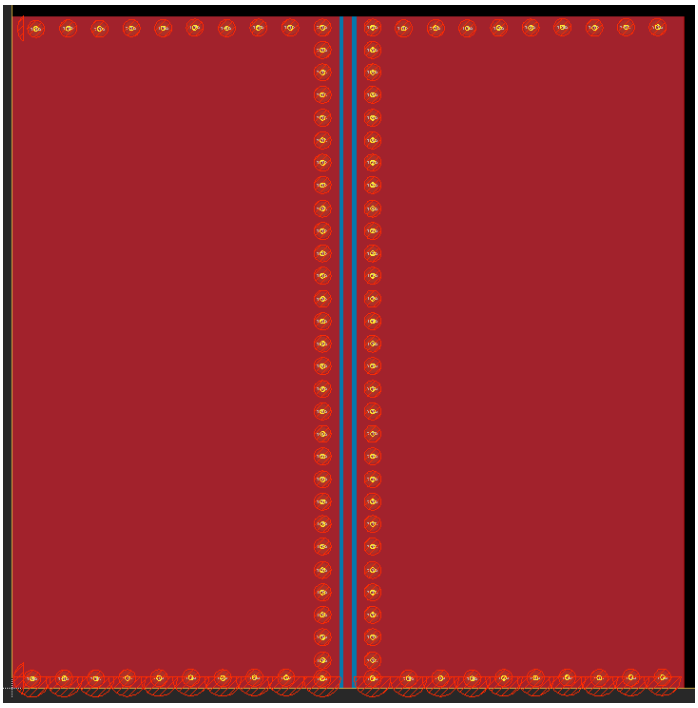

Figure B.5: **Microstrip CPW Schematic**: Depicted is a schematic in Fusion's EAGLE CAD program for designing electronics. The dimensions of the trace width are for the microstrip CPW, designed with 0.035 mm copper thickness and 1.00 mm substrate thickness. The AlN substrate is shown in blue, with the copper trace and upper groundplanes in red. Yellow vias (with red outline) are shown along three edges of the upper groundplanes, and connect through the substrate to the lower groundplane (not shown).

Prototype Measured Dimensions: Microstrip CPW					
Sample	**Trace Width 1 (mm)**	**Trace Width 2 (mm)**	**Gap Width 1 (mm)**	**Gap Width 2 (mm)**	**Trace Percent Difference**
A	0.353	0.355	0.238	0.224	6.84 %
B	0.385	0.381	0.184	0.195	0.74 %
C	0.379	0.379	0.195	0.194	0.33 %
D	0.391	0.390	0.187	0.190	2.79 %
E	-	-	-	-	- %
F	0.388	0.383	0.211	0.197	1.36 %

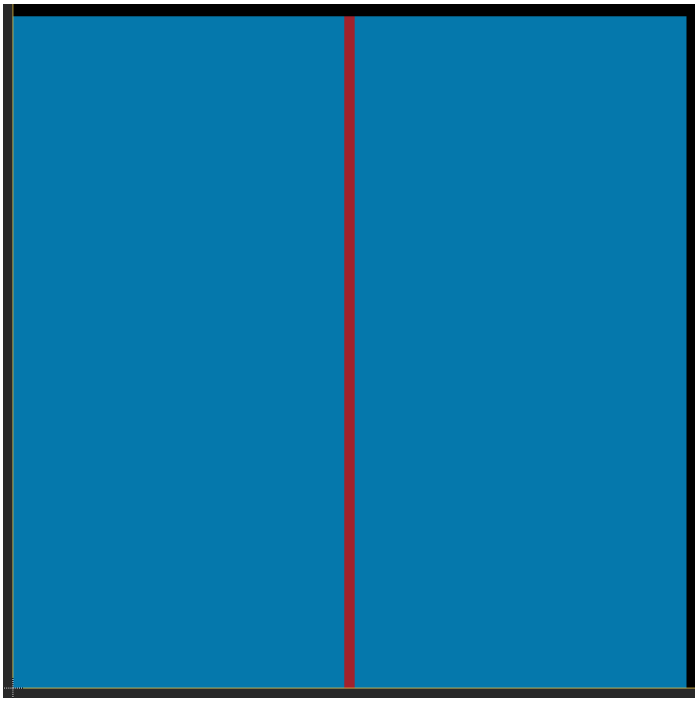

Figure B.6: **Microstrip Schematic**: Depicted is a schematic in Fusion's EAGLE CAD program for designing electronics. The dimensions of the trace width are for the microstrip, designed with 0.035 mm copper thickness and 0.038 mm substrate thickness. The AlN substrate is shown in blue, with the copper trace and upper groundplanes in red. Yellow vias (with red outline) are shown along three edges of the upper groundplanes, and connect through the substrate to the lower groundplane (not shown).

Prototype Measured Dimensions: Microstrip			
Sample	**Trace Width 1 (mm)**	**Trace Width 2 (mm)**	**Trace Percent Difference**
A	0.385	0.367	1.05 %
B	0.380	0.381	0.17 %
C	0.385	0.404	3.87 %
D	0.380	0.381	0.11 %
E	0.404	0.399	5.55 %
F	0.405	0.400	6.03 %