



## Monolithic N-Channel JFET Dual

PRODUCT SUMMARY				
$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	$g_{fs}$ Min (mS)	$I_G$ Max (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
-1.0 to -4.5	-50	1	-50	25

### FEATURES

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 5 pA
- Low Noise: 9 nV/√Hz
- High CMRR: 100 dB

### BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

### APPLICATIONS

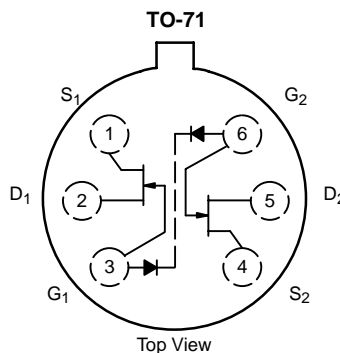
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

### DESCRIPTION

The low cost 2N3958 JFET dual is designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This series features tightly matched specs, low gate leakage for accuracy, and wide dynamic range with  $I_G$  guaranteed at  $V_{DG} = 20$  V.

The hermetically-sealed TO-71 package is available with full military processing (see Military Information and the 2N5545/5546/5547JANTX/JANTXV data sheet).

For similar products see 2N5196/5197/5198/5199, the low-noise U/SST401 series, the high-gain 2N5911/5912, and the low-leakage U421/423 data sheets.



### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage ..... -50 V  
 Gate Current ..... 50 mA  
 Lead Temperature ( $1/16$ " from case for 10 sec.) ..... 300 °C  
 Storage Temperature ..... -65 to 200 °C  
 Operating Junction Temperature ..... -55 to 150 °C

Power Dissipation : Per Side<sup>a</sup> ..... 250 mW  
 Total<sup>b</sup> ..... 500 mW

Notes  
 a. Derate 2 mW/°C above 85 °C  
 b. Derate 4 mW/°C above 85 °C

SPECIFICATIONS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ <sup>a</sup>	Max	
<b>Static</b>						
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V	-50	-57		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 1 nA	-1.0	-2	-4.5	
Saturation Drain Current <sup>b</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	0.5	3	5	mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V		-10	-100	pA
		T <sub>A</sub> = 150 °C		-20	-500	nA
Gate Operating Current	I <sub>G</sub>	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA		-5	-50	pA
		T <sub>A</sub> = 125 °C		-0.8	-250	nA
Gate-Source Voltage	V <sub>GS</sub>	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA	-0.5	-1.5	-4	V
		I <sub>D</sub> = 50 μA			-4.2	
Gate-Source Forward Voltage	V <sub>GS(F)</sub>	I <sub>G</sub> = 1 mA, V <sub>DS</sub> = 0 V			2	
<b>Dynamic</b>						
Common-Source Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V f = 1 kHz	1	2.5	3	mS
Common-Source Output Conductance	g <sub>os</sub>			2	35	μS
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V f = 1 MHz		3	4	pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>			1	1.2	
Drain-Gate Capacitance	C <sub>dg</sub>	V <sub>DG</sub> = 10 V, I <sub>S</sub> = 0, f = 1 MHz			1.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 kHz		9		nV/ √Hz
Noise Figure	NF	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V f = 100 Hz, R <sub>G</sub> = 10 MΩ			0.5	dB
<b>Matching</b>						
Differential Gate-Source Voltage	V <sub>GS1</sub> - V <sub>GS2</sub>	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA		15	25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA T <sub>A</sub> = -55 to 125 °C		20	100	μV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	0.85	0.97	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 200 μA f = 1 kHz	0.85	0.97	1	
Differential Output Conductance	g <sub>os1</sub> - g <sub>os2</sub>				0.1	
Differential Gate Current	I <sub>G1</sub> - I <sub>G2</sub>	V <sub>DG</sub> = 20 V, I <sub>D</sub> = 200 μA T <sub>A</sub> = 125 °C		0.1	10	nA
Common Mode Rejection Ratio <sup>c</sup>	CMRR	V <sub>DG</sub> = 10 to 20 V, I <sub>D</sub> = 200 μA		100		dB

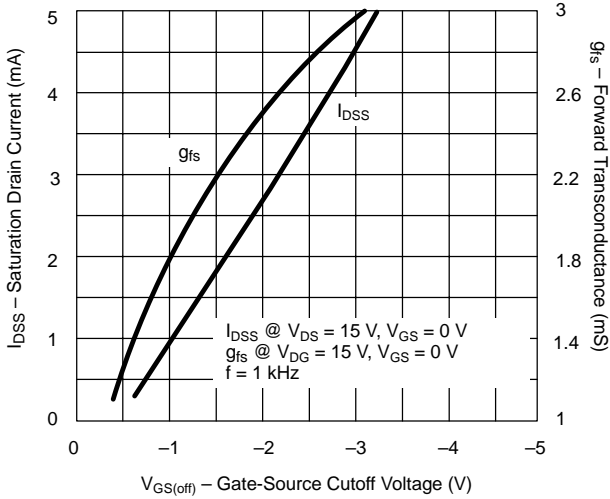
## Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
 b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.  
 c. This parameter not registered with JEDEC.

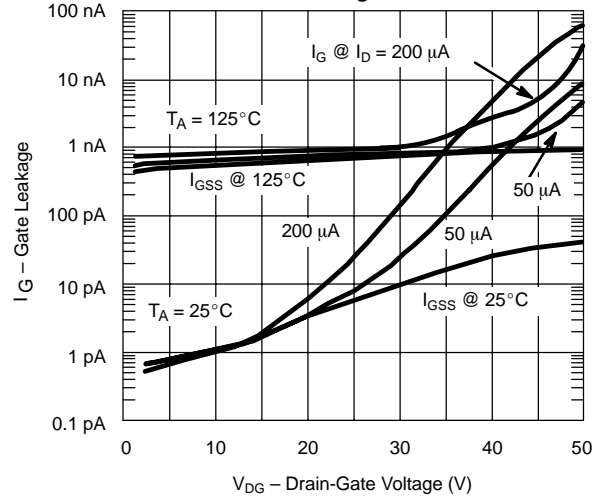
NQP

**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

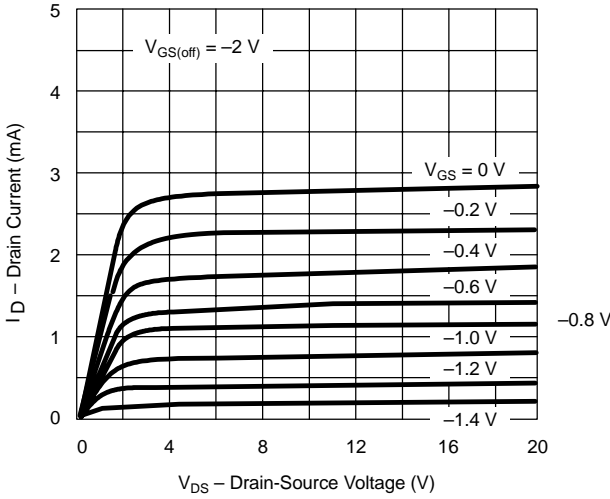
**Drain Current and Transconductance vs. Gate-Source Cutoff Voltage**



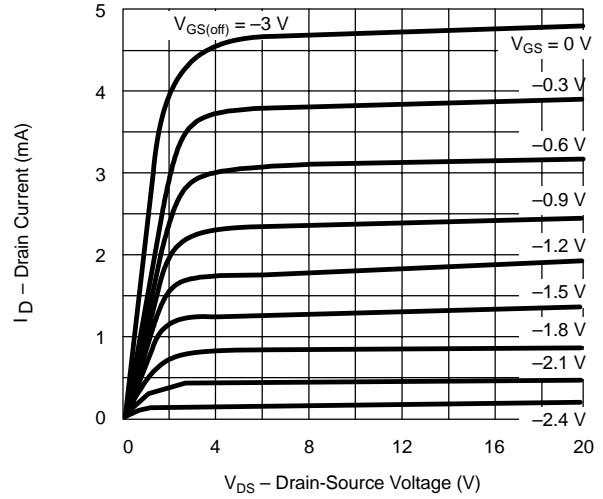
**Gate Leakage Current**



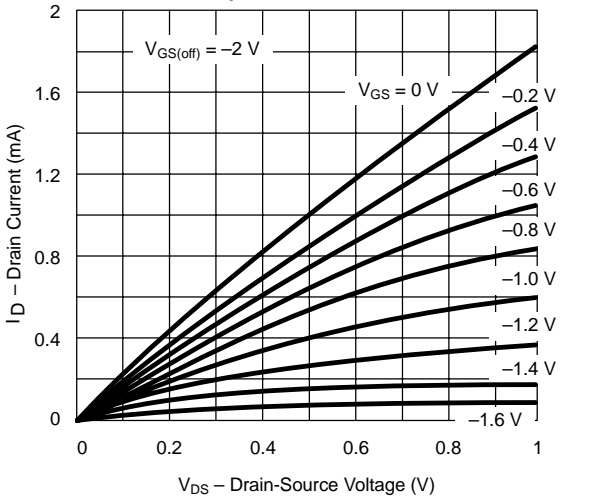
**Output Characteristics**



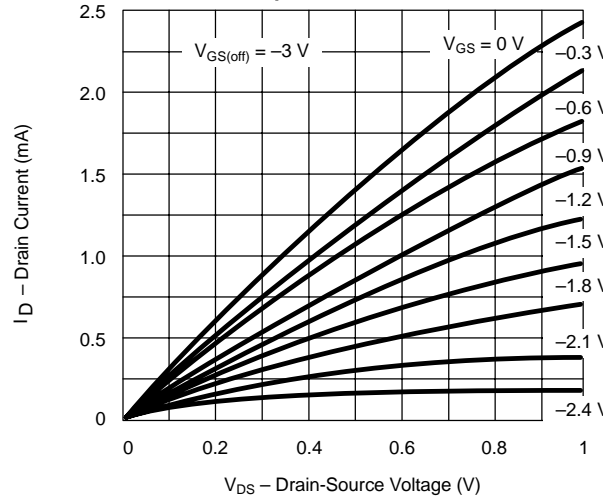
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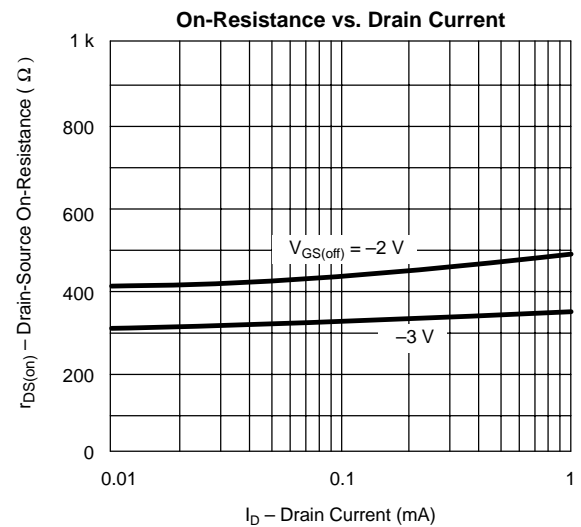
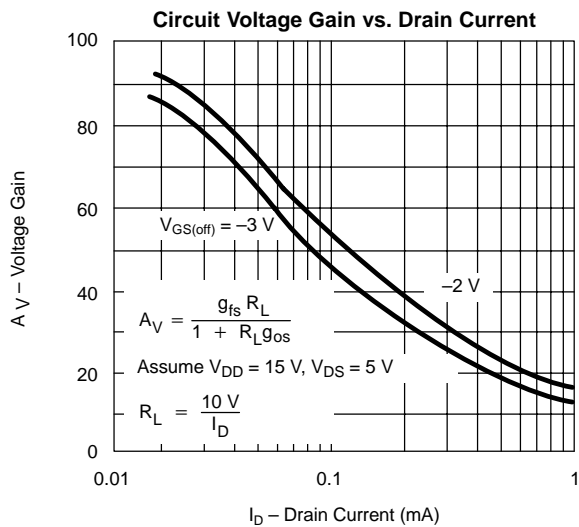
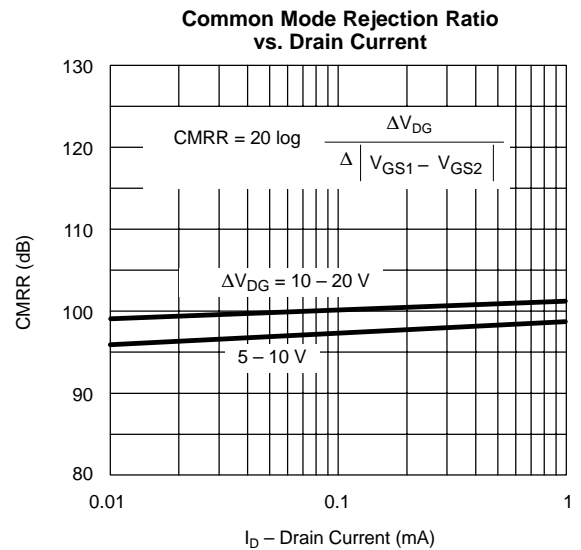
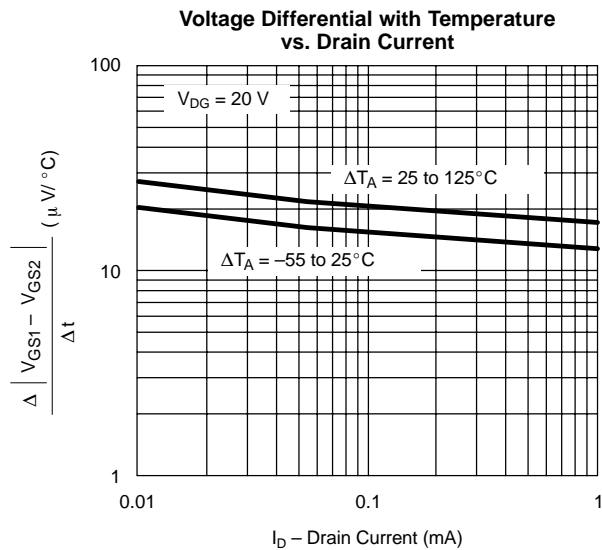
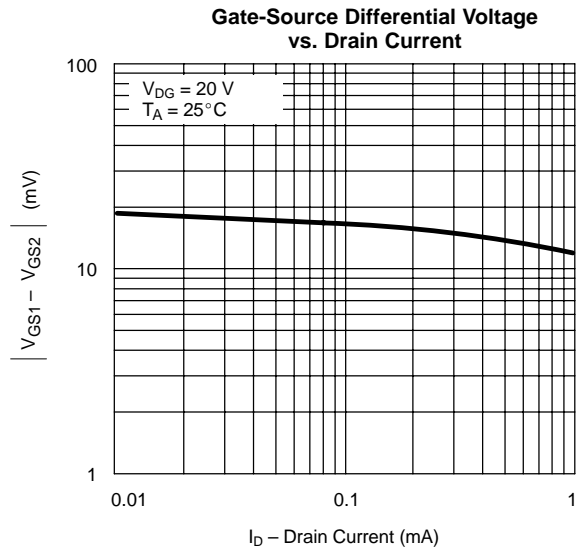
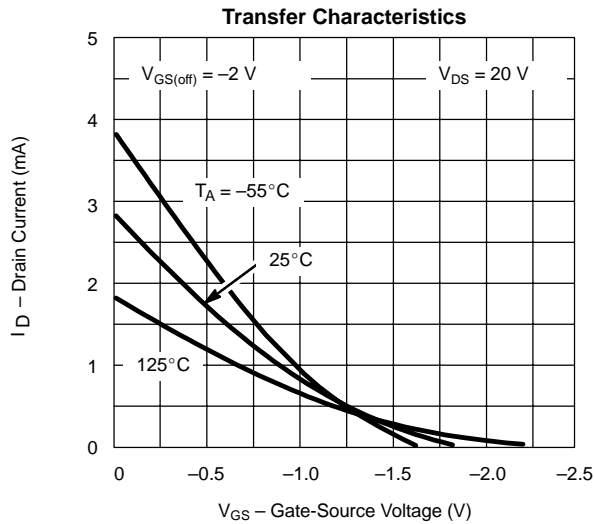
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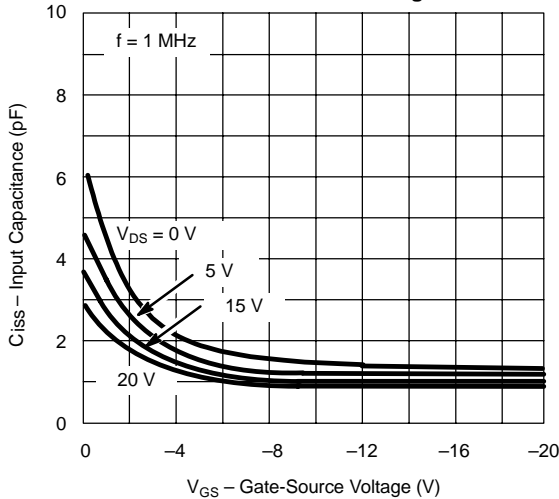
**TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)**



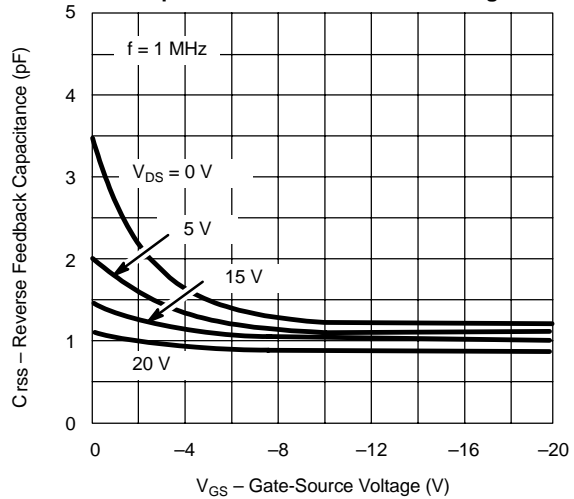


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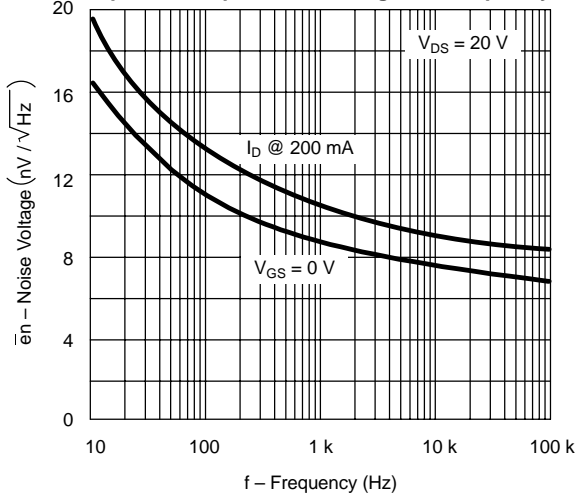
**Common-Source Input Capacitance vs. Gate-Source Voltage**



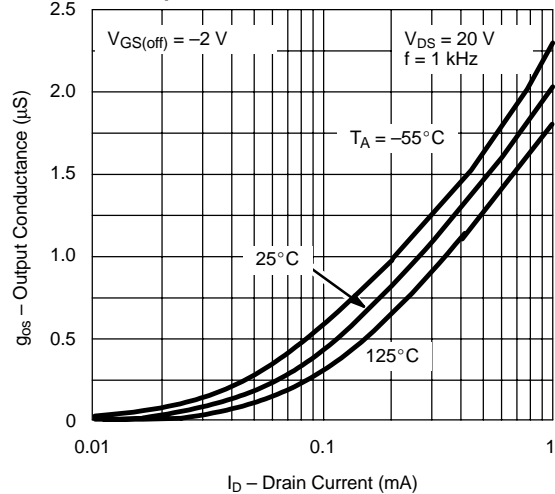
**Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage**



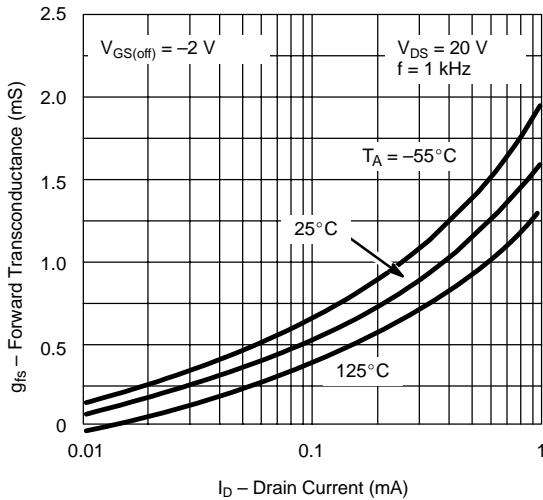
**Equivalent Input Noise Voltage vs. Frequency**



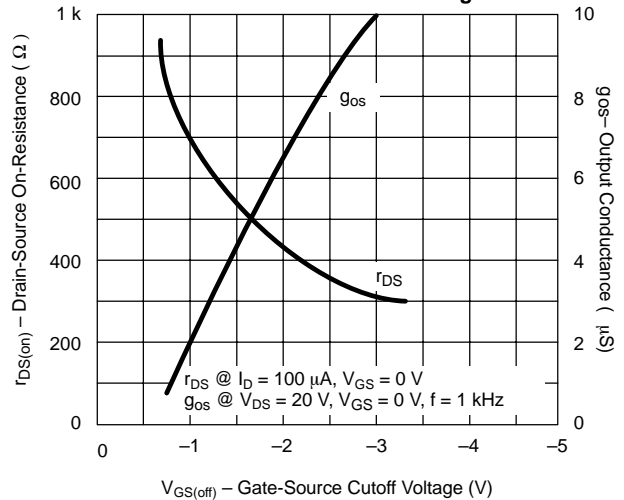
**Output Conductance vs. Drain Current**



**Common-Source Forward Transconductance vs. Drain Current**



**On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage**





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