Matched N-Channel JFET Pairs

PRODUCT SUMMARY

| Part Number | \( V_{G\text{S\text{off}}} \) (V) | \( V_{(B\text{R})\text{GSS}} \) Min (V) | \( g_{fs} \) Min (mS) | \( I_G \) Typ (pA) | \( |V_{GS1} - V_{GS2}| \) Max (mV) |
|-------------|-------------------------------|---------------------------------|----------------|----------------|-------------------------------|
| U440        | –1 to –6                       | –25                             | 4.5            | –1             | 10                            |
| U441        | –1 to –6                       | –25                             | 4.5            | –1             | 20                            |

FEATURES

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 85 dB.

BENEFITS

- Minimum Parasitics Ensuring Maximum High-Frequency Performance
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

DESCRIPTION

The U440/441 are matched pairs of JFETs mounted in a single TO-71 package. This two-chip design reduces parasitics and gives better performance at very high frequencies while ensuring extremely tight matching. These devices are an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications.

The hermetically-sealed TO-71 package is available with full military screening per MIL-S-19500 (see Military Information).

For similar products in SO-8 packaging see the SST440/SST441 data sheet. For low-noise options, see the SST/U401 series data sheet. For low-leakage alternatives, see the U421/423 data sheet.

ABSOLUTE MAXIMUM RATINGS

- Gate-Drain, Gate-Source Voltage: \(-25\) V
- Gate-Gate Voltage: \(\pm 50\) V
- Gate Current: 50 mA
- Lead Temperature ( \(1/16\)” from case for 10 sec.): 300°C
- Storage Temperature: \(-65\) to 200°C
- Operating Junction Temperature: \(-55\) to 150°C
- Power Dissipation:
  - Per Side\(^a\): 250 mW
  - Total\(^b\): 500 mW

Notes:

- Derate 2 mW/°C above 25°C
- Derate 4 mW/°C above 25°C
# SPECIFICATIONS (TA = 25°C UNLESS OTHERWISE NOTED)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Typa</th>
<th>Min</th>
<th>Max</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static</strong></td>
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<td></td>
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</tr>
<tr>
<td>Gate-Source Cutoff Voltage</td>
<td>V_{GS(off)}</td>
<td>V_DS = 10 V, I_D = 1 mA</td>
<td>–3.5</td>
<td>–1</td>
<td>–1</td>
<td>–1</td>
<td>–6</td>
<td>–6</td>
</tr>
<tr>
<td>Saturation Drain Currentb</td>
<td>I_{DSS}</td>
<td>V_DS = 10 V, V_GS = 0 V</td>
<td>15</td>
<td>6</td>
<td>30</td>
<td>6</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>Gate Reverse Current</td>
<td>I_{GSS}</td>
<td>V_GS = –15 V, V_DS = 0 V</td>
<td>–1</td>
<td>–500</td>
<td>–500</td>
<td>–500</td>
<td>–500</td>
<td>pA</td>
</tr>
<tr>
<td>Gate Operating Current</td>
<td>I_G</td>
<td>V_DG = 10 V, I_D = 5 mA</td>
<td>–1</td>
<td>–500</td>
<td>–500</td>
<td>–500</td>
<td>–500</td>
<td>nA</td>
</tr>
<tr>
<td>Gate-Source Forward Voltage</td>
<td>V_{GS(F)}</td>
<td>I_G = 1 mA, V_DS = 0 V</td>
<td>0.7</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td><strong>Dynamic</strong></td>
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</tr>
<tr>
<td>Common-Source Forward Transconductance</td>
<td>g_{fs}</td>
<td>V_DS = 10 V, I_D = 5 mA</td>
<td>6</td>
<td>4.5</td>
<td>9</td>
<td>4.5</td>
<td>9</td>
<td>mS</td>
</tr>
<tr>
<td>Common-Source Output Conductance</td>
<td>g_{os}</td>
<td></td>
<td>70</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>μS</td>
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<tr>
<td>Common-Source Input Capacitance</td>
<td>C_{iss}</td>
<td>V_DS = 10 V, I_D = 5 mA</td>
<td>3</td>
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<td></td>
<td></td>
<td></td>
<td>pF</td>
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<tr>
<td>Common-Source Reverse Transfer Capacitance</td>
<td>C_{rss}</td>
<td>V_DS = 10 V, I_D = 5 mA, f = 1 MHz</td>
<td>1</td>
<td></td>
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<tr>
<td>Equivalent Input Noise Voltage</td>
<td>\bar{\theta}_{n}</td>
<td>V_DS = 10 V, I_D = 5 mA, f = 10 kHz</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td><strong>Matching</strong></td>
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<tr>
<td>Differential Gate-Source Voltage</td>
<td></td>
<td>V_DG = 10 V, I_D = 5 mA</td>
<td>6</td>
<td>10</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>mV</td>
</tr>
<tr>
<td>Gate-Source Voltage Differential Change with Temperature</td>
<td>\Delta V_{GS1} – V_{GS2}</td>
<td>V_DG = 10 V, I_D = 5 mA, T_A = –55 to 125°C</td>
<td>20.0</td>
<td>20.0</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Saturation Drain Current Ratio^c</td>
<td>I_{DSS1} / I_{DSS2}</td>
<td>V_DS = 10 V, V_GS = 0 V</td>
<td>0.97</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transconductance Ratio^c</td>
<td>g_{fs1} / g_{fs2}</td>
<td>V_DS = 10 V, I_D = 5 mA, f = 1 kHz</td>
<td>0.97</td>
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<td></td>
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<tr>
<td>Common Mode Rejection Ratio</td>
<td>CMRR</td>
<td>V_DG = 5 to 10 V, I_D = 5 mA</td>
<td>85</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

Notes:

a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤300 μs duty cycle ≤3%.
c. Assumes smaller value in the numerator.
**TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)**

**Drain Current and Transconductance vs. Gate-Source Cutoff Voltage**

- $I_{DSS} @ V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}$
- $g_{fs} @ V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}$
- $f = 1 \text{ kHz}$

**Gate Leakage Current**

- $I_{G(on)} @ I_D$
- $I_{GSS} @ 25 \text{ °C}$
- $T_A = 125 \text{ °C}$
- $I_D = 10 \text{ mA}$

**Output Characteristics**

- $V_{GS} = 0 \text{ V}$
- $V_{GS} = 0 \text{ V}$
- $V_{GS} = 0 \text{ V}$
- $V_{GS} = 0 \text{ V}$

**Saturation Drain Current ($I_{DSS}$)**

- $0.1 \text{ pA}$
- $1 \text{ pA}$
- $10 \text{ pA}$
- $1 \text{ mA}$

**Saturation Drain Current ($I_{DSS}$)**

- $40 \text{ mA}$
- $10 \text{ mA}$
- $1 \text{ mA}$
- $10 \text{ mA}$
TYPICAL CHARACTERISTICS (TA = 25°C UNLESS OTHERWISE NOTED)

- **Transfer Characteristics**
  - **Gate-Source Voltage (V)** vs. **Drain Current (mA)**
  - **Gate-Source Voltage (V)** vs. **Forward Transconductance (mS)**
  - **Voltage Gain** vs. **Drain Current (mA)**
  - **On-Resistance vs. Drain Current**

- **Transfer Characteristics** (TA = 25°C, VGS(off) = -2 V, VDS = 10 V)
- **Transconductance vs. Gate-Source Voltage** (TA = -55°C, VGS(off) = -2 V, f = 1 kHz)
- **Circuit Voltage Gain vs. Drain Current**
  - Assume VDD = 15 V, VDS = 5 V

- **On-Resistance vs. Drain Current**
  - VGS(off) = -5 V

**Note:** The document includes detailed graphs and equations for various electrical characteristics of the device, such as drain current, voltage gain, and on-resistance.
TYPICAL CHARACTERISTICS (TA = 25°C UNLESS OTHERWISE NOTED)

Common-Source Input Capacitance vs. Gate-Source Voltage

Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage

Input Admittance

Forward Admittance

Reverse Admittance

Output Admittance
TYPICAL CHARACTERISTICS (\(T_A = 25^\circ C\) UNLESS OTHERWISE NOTED)

- **Equivalent Input Noise Voltage vs. Frequency**
  - \(V_{DS} = 10\) V
  - \(I_D = 1\) mA
  - \(I_D = 10\) mA

- **Output Conductance vs. Drain Current**
  - \(V_{DS(drain)} = -5\) V
  - \(V_{DS} = 10\) V
  - \(V_{DS} = 25\) V
  - \(I_D\) Drain Current (mA)

- **On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage**
  - \(r_{DS(on)} @ I_D = 1\) mA, \(V_{GS} = 0\) V
  - \(g_{os} @ V_{DS} = 10\) V, \(V_{GS} = 0\) V
  - \(f = 1\) kHz

- **Common-Source Forward Transconductance vs. Drain Current**
  - \(V_{GS(sink)} = -5\) V
  - \(V_{DS} = 10\) V
  - \(T_A = -55^\circ C\)
  - \(I_D\) Drain Current (mA)
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