

Chapter 8: Field Effect Transistors

Transistors are different from the basic electronic elements in that they have three terminals. Consequently, we need more parameters to describe their behavior than one simple current-voltage characteristic. We found that thinking of the transistor as a current amplifier was a particularly useful model. This model, however, does have its limitations and we could extend it.

A next step would be a *transconductance* model, such the Ebers-Moll model. In this improved model, the collector current depends on the base-emitter *voltage*, so that V_{BE} produces I_C . In this model, V_{BE} also produces I_B so this model includes the earlier current amplifier model in addition to the new features.

I. Field-Effect Transistors

A. Introduction to FETs

This week's we introduce a new element called a *Field-Effect Transistor (FET)*. It is also a three-terminal element. The three terminals are similar to the transistor's base, emitter and collector, but they are called the *gate*, *source* and *drain*. The initial FETs we will use (the 2N5485) have identical packages to the transistors we used in earlier in the semester. The schematic symbol for the FETs we will use are shown in figure 8.1 on the right.

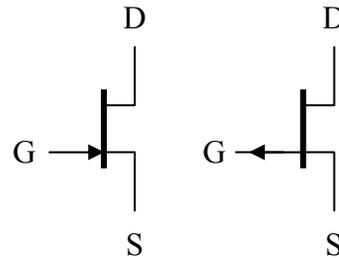


Figure 8.1: An n-channel JFET (left) and a p-channel JFET (right).

A FET is produced from a single piece of conducting silicon that connects to the source and the drain. This is called the *channel*. The gate is then created by diffusing a third connection, the gate. A voltage applied to the gate controls the conductivity of the channel.

The gate-channel junction looks like a diode that never conducts hence the gate draws no current. This is the major difference between normal transistors and FETs. Consequently FETs have extremely large gate input impedances ($>10^{12}\Omega$). Thus, we will be forced from the start into modeling the device with a transconductance model where the drain current depends on the gate voltage and not the current. This is the major difference between the bipolar diodes that we used previously and FETs.

FETs are extremely important as input stages to amplifiers. Since they have such a large input impedances that they almost attain the ideal of measuring a voltage without drawing any current from the source. This is great if you want to measure small charges deposited on capacitors – as you might want to do in a particle detector.

FETs come in five general types, but we will restrict ourselves to JFETs (for Junction FET) initially and our examples will only use n -channel JFETs. These have n channel doping and are similar to nnp transistors. The p channel JFET requires the opposite voltage on the gate. They usually have poorer performance due to the lower mobility and shorter lifetimes of holes, as compared to electrons.

As mentioned above, the source-drain current is the only current that flows through a FET. The source-drain current is labeled I_D . The voltage applied to the gate terminal enables this current by creating an electric field inside the channel. There is no fundamental difference between the source and drain terminals of a JFET. The gate-drain capacitance, however, is usually lower than the gate-source capacitance so they are usually used as specified. This makes it different from a normal transistor, since current can flow either from the drain to the source or from the source to the drain.

Note that there is a maximum value and a minimum value for the gate voltage in order to keep the device operating. Since a JFET has a diode junction separating the gate from the channel, the gate must be held at a voltage of less than 0.6 V above the channel (usually the source terminal). If the gate voltage becomes greater than this, the junction will become conducting and the gate current will no longer be zero. Usually, we will not let the voltage between the gate and the source (V_{GS}) get any greater than 0. If the gate is biased too negative then no current flows and the channel is said to be “pinched off.” This minimum gate voltage, called V_p , is a characteristic that varies from one model of JFET to the next. It is usually in the range from -3 V to -10 V. Even within the same type of FET this parameter varies significantly from one device to the next. For example, the range specified for a 2N5485 the range is between -0.3 V and -3.0 V.

Let’s summarize these properties:

$$\text{For } V_{GS} < V_p: \quad I_D = 0 \quad (8.1)$$

$$\text{For } V_{GS} > 0.6 \text{ V: Device Fails!} \quad (8.2)$$

When V_{GS} is between these bounds I_D depends on both V_{GS} and V_{DS} . A complete description of the device would require a two-dimensional plot showing how I_D varies with both V_{GS} and V_{DS} .

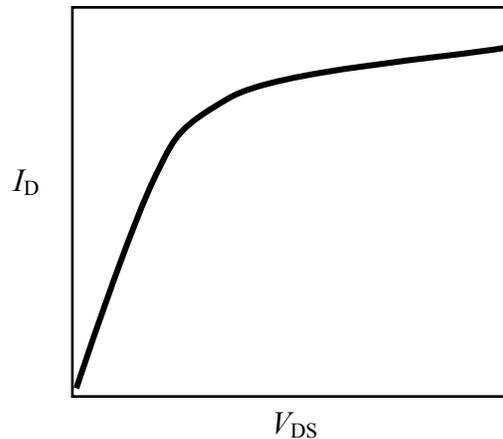


Figure 8.2: A sketch of drain current versus channel voltage.

B. Regions of Operation

For a fixed V_{GS} , the basic behavior of the drain current as a function of the channel voltage is shown in Figure 8.2 above. The behavior can be simply modeled in two regions. For small values of V_{DS} , I_D is almost proportional to V_{DS} just like a resistor. This is called the *linear region*. For reasonably large values of V_{DS} , I_D has little dependence on V_{DS} . This is called the *saturation region*. The actual relationships and conditions can be approximated as:

For $V_{DS} < V_{GS} - V_P$: $I_D = k [2(V_{GS} - V_P)V_{DS} - V_{DS}^2]$ Linear Region (8.3)

For $V_{DS} > V_{GS} - V_P$: $I_D = k (V_{GS} - V_P)^2$ Saturation Region (8.4)

For small enough voltages the quadratic term is small. In this case, the current in the linear region is proportional to V_{DS} just like a resistor. This is true even for negative V_{DS} . Since I_D is proportional to both V_{GS} and V_{DS} this gives us a way to make voltage-controlled resistors. Moreover, since I_D is proportional to both V_{DS} and V_{GS} , we can generate a current corresponding to the product of two signals.

In the saturated region I_D is nearly independent of V_{DS} . We can use this to make excellent current sources and source followers. This is similar to our transistor-based emitter follower but with a much larger input impedance. Note that in this region there is still a small slope and this slope increases for larger gate voltages. We will discuss the saturated region later in the chapter.

C. A Voltage Controlled Resistor

From Equation 8.3 we can see that the drain current is proportional to V_{DS} , when V_{DS} is small, and the proportionality constant is proportional to V_{GS} . This is perfect for making a voltage-controlled resistor. A typical data sheet will list $R_{D(ON)}$ as the resistance measured when the gate is shorted to the source. From Equation 8.3 we see that $R_{D(ON)}$ is approximately $-1/2kV_P$. If you put this “resistor” in series with a fixed resistor, then you will have a voltage-controlled attenuator. If this follows or precedes an amplifier the combination would be an amplifier with a voltage-controlled gain.

The resistor R_D and the FET in Figure 8.3 form a voltage divider to attenuate the input voltage. The size of the equivalent resistance of the FET is determined by V_{GS} , which is set by the potentiometer.

By making the right choice of gate voltages we can improve the circuit by eliminating the quadratic term in Equation 8.3 and thus improving the linearity of the attenuator. From Equation 8.3 we see that

$$1/R_{DS} = I_D / V_{DS}$$

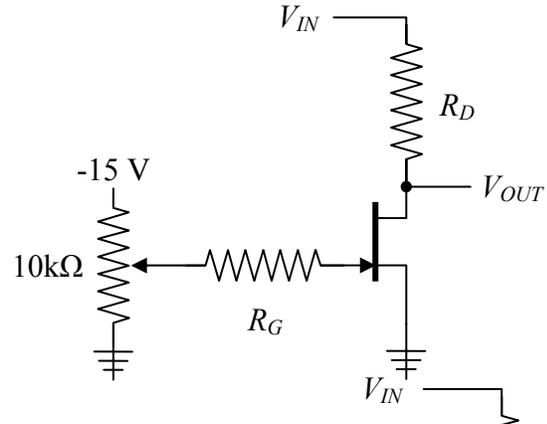


Figure 8.3: Uncompensated voltage-divider.

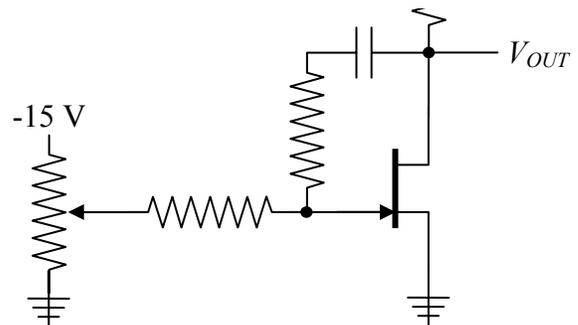


Figure 8.4: Compensated voltage-divider.

$$= k [2(V_{GS} - V_P) - V_{DS}] \quad (8.5)$$

If we set V_{GS} to exactly $V_{DS}/2$ then we find

$$R_{DS} = -1/(2kV_P) \quad (8.6)$$

Figure 4 shows a version of the attenuator that employs this improved linearity. The two resistors connected to the gate force half of the drain voltage onto the gate. They should be much larger than the potentiometer. The capacitor just blocks DC so that only the signal part of the input voltage is fed to the gate.

Application: Amplitude Modulator

If you feed a second, lower frequency, signal into the gate in addition to the DC voltage from the potentiometer, then you can modulate the attenuation of your voltage divider. Of course, you should feed this in via a capacitor so that you do not disturb the quiescent (DC) conditions.

II. The Saturated Region

As we saw in equation 4, for large values of V_{DS} the drain current only depends on V_{GS} :

$$I_D = k (V_{GS} - V_P)^2 \quad (8.7)$$

This saturation is useful, for example, for making current sources and followers. As discussed earlier, there is still some dependence of I_D on V_{DS} even in the saturated region. You can, however, reduce this effect with a few extra tricks.

A. Transconductance

The *transconductance* of a FET is denoted by g_m and is defined as

$$g_m = \Delta I_D / \Delta V_{GS} \quad (8.8)$$

$$g_m \approx 2k (V_{GS} - V_P) \quad (8.9)$$

$$g_m = 2(kI_D)^{1/2} \quad (8.10)$$

The transconductance will be useful in understanding the behavior of the FET amplifiers.

You can interpret it as the slope of I_D vs V_{GS} in the saturated region and depends on your choice of I_D . A curve of $g_m(V_{GS})$ and $g_m(I_D)$ are usually shown in the data sheets and they have complicated shapes. If you know the value for one set of conditions you can use the above relationships to scale to other similar values.

The transconductance has units of Ω^{-1} which is known as a *mho* (pronounced “moe”). You often see the units of μmho (or umho pronounced “micro-moe”) for 10^{-6} mho and mmho (“milli-moe”) for 10^{-3} mho in FET specifications. You might also see an inverted capital omega or “S” to represent this unit.

The remainder of this section will cover some applications for FETs employing the saturated region.

B. JFET Current Sources

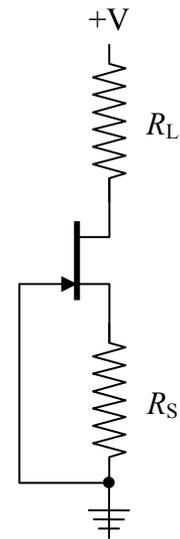
You can easily make a FET *current source* simply by connecting the gate to the source (i.e. $V_{GS} = 0$ V) and applying a high enough voltage to the drain that the JFET operates in the saturated region (Figure 1). This generates a current through the load. This specific current is I_{DSS} , where the subscript denotes that this is the drain current when the gate is shorted to the source.

According to the transconductance model given by equations 3 and 4, the saturation current, I_{DSS} , when $V_{GS} = 0$, is given by

$$I_{DSS} = kV_P^2 \quad (8.11)$$

Two-terminal JFETs, such as the 1N5294, are exactly this circuit packaged to look like a diode and sold under the name *current-regulator diodes*.

Since we know there are large variations in V_P this may not seem like the best specified device. In fact, when marketing these devices, a manufacturer will actually measure its response and only sell devices under this product type when they pass the roughly specified current (within a factor of two of 7 mA). This is called *preselection* and is common in some categories of commercial electronics production and also in devices with large variations such as photodetectors. Since this is expensive, the companies invest huge amounts into development on the more expensive components (e.g. CPU chips or disk drive heads) to improve quality control during fabrication.



You can make this circuit an adjustable or *programmable constant current source* by adding a resistor between the gate and source to provide an offset (Figure 5). Since there is a voltage drop across the resistor the current is given by

$$\begin{aligned} I_D &= k(V_{GS} - V_P)^2 \\ &= k(-R_S I_D - V_P)^2 \\ &= I_{DSS} \left(\frac{R_S I_D}{V_P} + 1 \right)^2 \end{aligned} \quad (8.12)$$

This can be solved for I_D but it is rather ugly. In practice, one normally starts from a plot of I_D vs V_{GS} on the device's data sheet to get a rough idea of the source resistor. Since the saturation properties are not well determined in the fabrication process (up to factors of 10), use a potentiometer if you wish to sink a specific current.

Figure 8.5: A programmable constant current source driving a load.

C. JFET Follower

The drain current in a JFET operating in the saturation region depends only on V_{GS} . Because of this, you can add a source resistor to a FET to provide a type of negative feedback. This is called a *source follower*.

In the follower's quiescent state there will be nominal values for I_D and V_{GS} . An increase in the gate voltage will increase the current into the source resistor. This will cause an increased voltage drop and act to raise the source voltage. It is conventional to use lower case letters to represent small variations from the quiescent point.

In our transconductance model, small variations would be governed by

$$i_d = g_m(v_g - v_s). \quad (8.13)$$

The source voltage is tied to the drop across the source resistor,

$$v_s = i_d R_S. \quad (8.14)$$

Solving these two equations, we find that

$$v_s = \frac{R_S g_m}{1 + R_S g_m} v_g = \frac{R_S}{1/g_m + R_S} v_g \quad (8.15)$$

For R_S much greater than $1/g_m$ we see that $v_g \approx v_s$ (i.e. gain = 1) and therefore this is a follower.

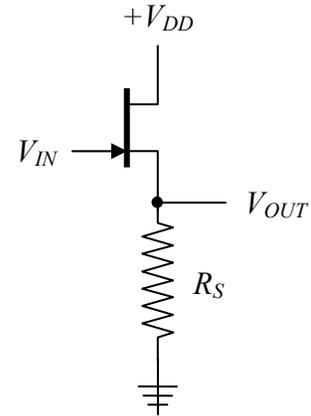


Figure 8.6: A simple source follower.

FET follower limitations

From Equation 9, we can see that the source follower acts like a voltage divider with the FET behaving like a resistor of $1/g_m$. Since it is a voltage divider we can determine its output impedance. Since the FET is the smaller resistor in the divider (or the output will not be very close to the gate), the output impedance of the source follower is just $1/g_m$, which is typically a few hundred ohms at currents of a few milliamps.

So, our simple follower, however, does not behave too well:

1. As V_{GS} varies, the nonlinear transconductance will distort the input.
2. It has quiescent output voltage that is specified by the pinch of voltage of the device and hence is unpredictable.
3. The required V_{GS} to produce a given quiescent current varies a lot from one device to the next
4. The output impedance is relatively high.

On the good side, the input impedance is immense.

A matched pair follower

A very common solution is to replace the ground at the end of the source resistor with a current source. This is called an *active load*. By putting in a constant current sink, we always have the same I_D and thus a fixed value for V_{GS} . The first problem is solved. It does not, however, fix the other problems.

We can do an even better job by noting manufacturing variations in FETs are significantly smaller for FETs made from the same piece of *silicon wafer*, or *die*. You can think of them as identical twins instead of just siblings. This is called a *matched pair*. The 2N3958 and U441 are examples of a matched pair JFETs.

Using the second JFET as the active load gets rid of most of the problems in the FET follower (Figure 7). The second JFET keeps the current constant, fixes V_{GS} , and eliminates the nonlinearities. The matched resistors also add better I_D predictability. Furthermore, when you use a matched FET pair and symmetric power supplies it largely eliminates the DC offset at the output. To fix the poor output impedance, one would need to add an op amp follower or amplifier to the output.

Matched pairs are used for the input stages of most charge measurement applications (e.g. oscilloscope inputs), sensitive electrometers, measurement of small charges (e.g. fC) like one sees in particle detectors, and current pre-amplifiers for photo-detectors.

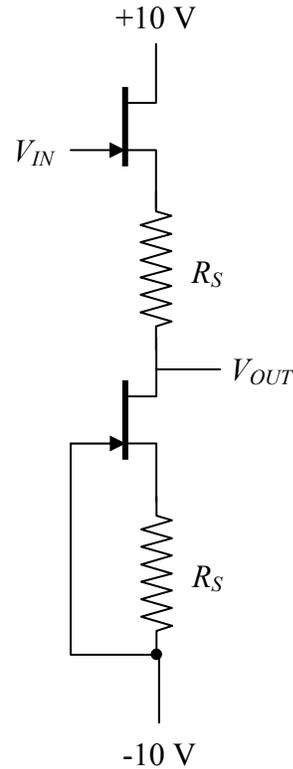


Figure 8.7: A matched pair follower.

Design Exercises

Design Exercise 8-1: Design a programmable current source with a design current of 1mA and a variable gate-source resistor. Pick a reasonable value based on the plot of I_D as a function of V_{GS} from the datasheet of a 2N5485.

Design Exercise 8-2: Determine the quiescent voltages (i.e. V_{GS} , V_S , and V_{DD}) and the quiescent power consumption for a source follower with $I_{DS}(\text{quiescent}) = 1 \text{ mA}$ and $R_S = 4.7 \text{ k}\Omega$. The N-JFET for the circuit has the following properties: $V_P = -2 \text{ V}$, $I_{DSS} = 3 \text{ mA}$, and $g_m = 2.5 \text{ mmhos}$.

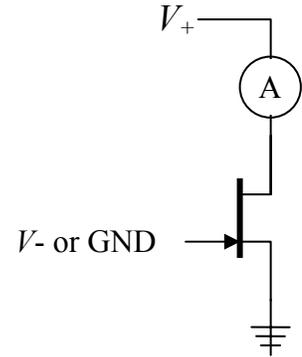
(*hint: Start by assuming that the circuit is operating in the saturation region and then choose V_{DD} at the end of the calculation to ensure that the FET is well into the saturation region.*)

Lab 8: Introduction to FETs

1. N-JFET Basics (1.5 hours)

a) Measure the characteristics of a 2N5485 *n*-channel JFET by measuring I_D versus V_{DS} while the gate is tied to the source (i.e. $V_{GS} = 0$). Construct a sketch as you make your measurements. Using the Formulas 1 and 2 from the text and data in the linear and saturated regions, compute V_P and k .

b) Measure the characteristics of the JFET by measuring I_D versus V_{DS} for an additional value of V_{GS} between V_P and ground. Does this agree with our model (i.e. does one value of k fit all your data)?



Do lab exercise 2 or 3.

2. Voltage controlled JFET attenuators (1.5 hours)

a) Construct an uncompensated attenuator with $R_D = 10\text{ K}\Omega$. Use a voltage divider with your variable -15 V supply to generate the V_{GS} control voltage in the approximate range of -0.5 V to -5 V . Connect the output of the voltage divider to the gate through a $1\text{ M}\Omega$ gate resistor. Try to attenuate your input by a factor of 10 using this device when you drive the drain with a small signal ($<1\text{ V}$) around 1 kHz . Note that this attenuator even works for the negative values of V_{DS} function generator. Check for distortion using the FFT feature on the oscilloscope.

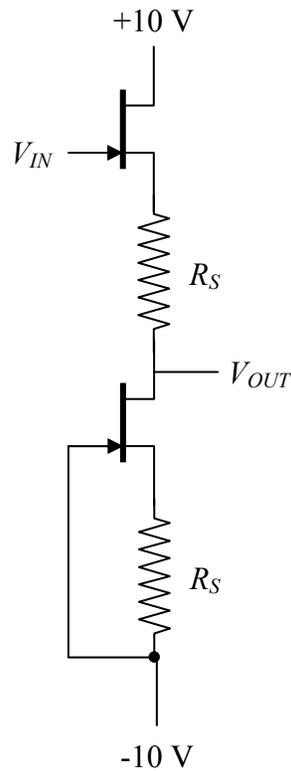
b) Now compensate your attenuator using a second $1\text{ M}\Omega$ feedback resistor between the drain and the gate. Use a $\sim 0.1\text{ }\mu\text{F}$ capacitor to block the DC drain voltage. Measure the new attenuation and distortion. How do the new characteristics compare to the uncompensated ones?

c) Connect the signal from another function generator to the voltage divider to form a bias-T using another capacitor. Set this frequency to be roughly 10 times lower than the frequency on the drain. Use small AC inputs for both signals (tenths of volts) and describe the output. Describe the signal in the time domain and in frequency space. Do your results agree with theory? What arithmetic operation does your circuit implement on the two input signals?

3. Matched-pair source-follower (1.5 hours)

a) Construct a simple source follower with a 2N3958 (or U441) JFET. Use a $4.7\text{ k}\Omega$ source resistor. Using a small sine wave around 1 kHz, measure its gain and DC offset. Estimate g_m from the attenuation. Measure its output impedance. Do they agree?

b) Add an active load to your source follower using the second JFET from the matched pair. Measure its new gain, its DC offset and its output impedance.



A matched-pair follower