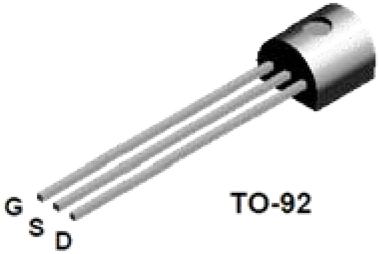
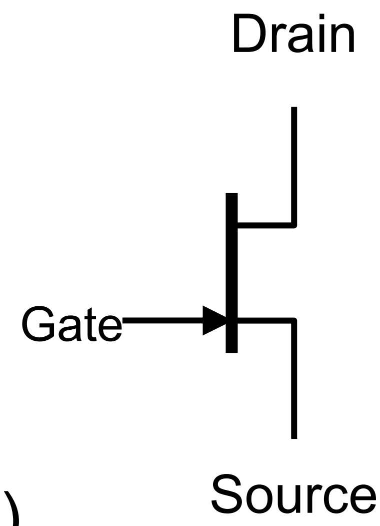
Transistors III: FETs

- 3-terminal device like a BJT

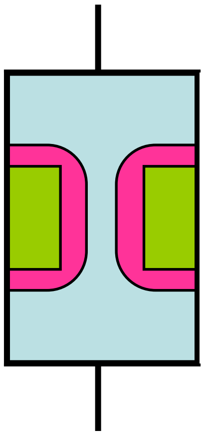


- New names for the connections
  - **Drain** (input) …sort of like collector
  - **Source** (output) … sort of like emitter
  - **Gate** (controls flow) … sort of like base



- 2 broad types
  - Junction FETs (JFETs)
  - Metal-oxide-semiconductor (MOSFETs)

Principle of Operation



- Made from a conducting piece of silicon
  - This is called the ***channel***
  - ***Drain*** on one end
  - ***Source*** on the other
  - In the middle a **gate** is embedded
- Current regulation
  - If the gate is at a negative voltage there is a charge **depletion zone** around the gate
    - Current cannot flow in this zone
    - Expands as the gate becomes more negative
  - Controls the conductivity of the channel
- At a **pinch off voltage** the current stops (V_p)
  - Think of pinching a hose to cut off the flow of water

JFETs vs. MOSFETs

- JFET gate forms a diode junction with the channel. Input impedance ~ 10^{12} Ω.

- MOSFET has a insulating layer for better input impedance (up to 10^{14}Ω).

- MOSFETs have an extra terminal called the **body.**
  → Usually just connected to the source to remove charge.

- MOSFETs are generally used for power circuits and digital circuits.

- Many other types now available.

FETs vs. BJTs

FET Pros

- The gate of a FET draws almost no current (i.e. pA range).
- FETs have almost infinite input impedance.
- Can frequently make a better amplifier circuit with a FET.
- Can operate bi-directionally sometimes.

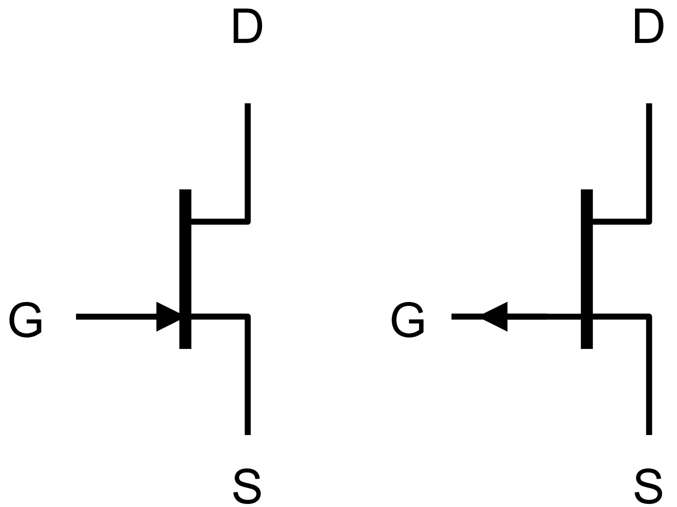
FET cons

- FETs are more complicated than BJTs

  → complicated operational model.
- FET have even larger parameter spreads than BJTs.

FET properties

- Can be a n-channel or a p-channel
  - **N-channel** like *npn*
  - **P-channel** like *pnp*
- Gate may be centered on some diagrams
  - Have to figure out it which is which from "context"
  - Source & Drain are nearly identical
  - Can be used backwards with almost same performance
- **N-channel** usually faster than **P-channel** due to higher mobility of electrons vs holes moving in the channel.



n-channel JFET (left)
p-channel JFET (right)

Gate Voltage Rules

V_p = pinch-off voltage: this is an intrinsic parameter of the JFET.

- $V_{GS} < V_p$

  → $I_D = 0$

- For $V_{GS} > 0.6$ V

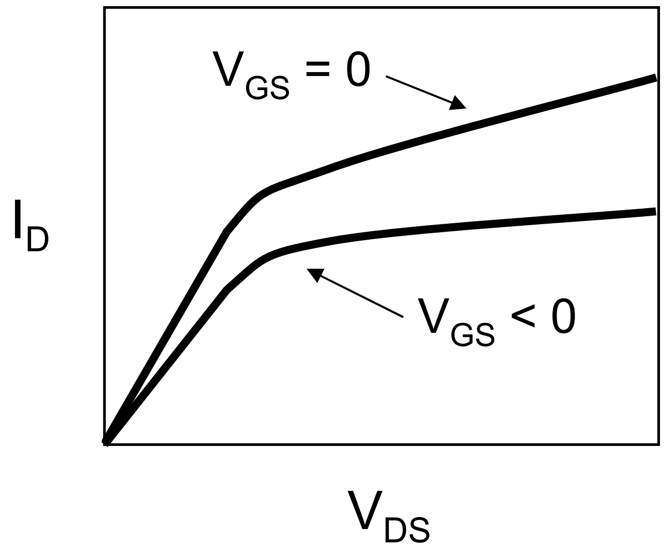
  → Device Fails!!!

  → Try to keep $V_{GS}<0$

- $V_p < V_{GS} < 0.6$ V

  → I_D depends on both V_{GS} & V_{DS}

  → A complete description would require a 2D function: $I_D(V_{GS}, V_{DS})$

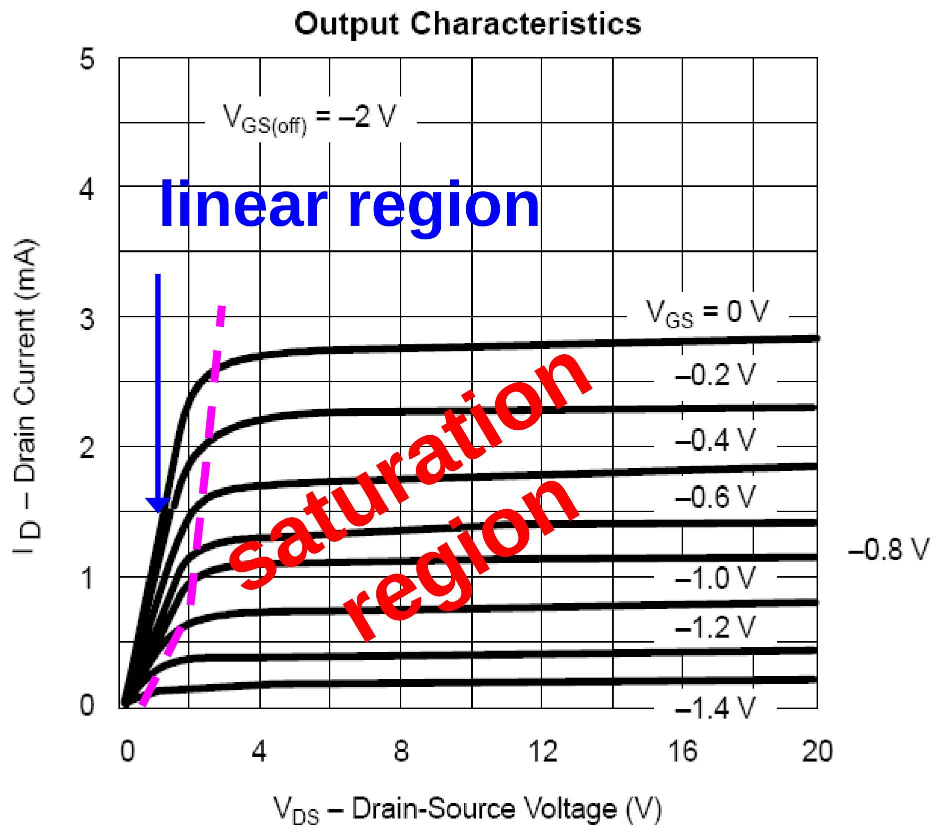


Linear and Saturation Regions

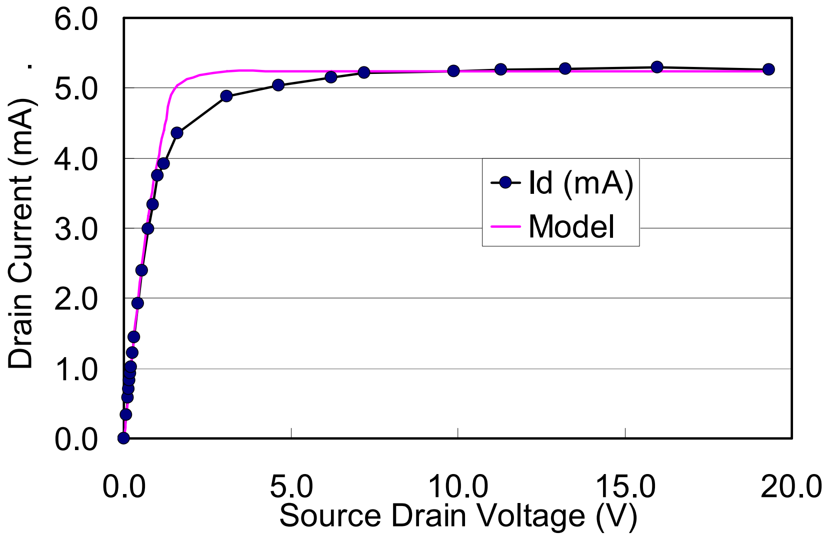
$$\text{Linear Region}: V_{DS} < V_{GS} - V_P$$
$$\rightarrow \quad I_D = k\,[\,2(V_{GS} - V_P)V_{DS} - V_{DS}^{\,2}\,]$$

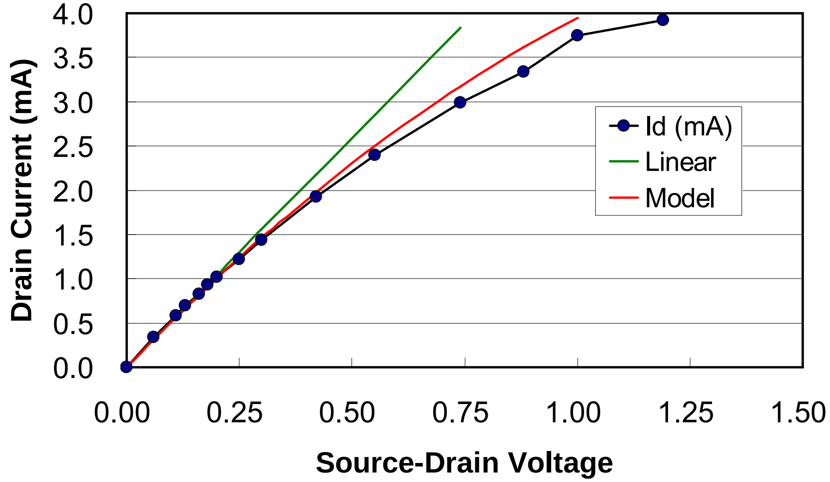
$$\text{Saturation Region}: V_{DS} > V_{GS} - V_P$$
$$\rightarrow \quad I_D = k\,(V_{GS} - V_P)^2$$

- V_p is the **pinch-off** voltage
  → It's negative for n-channel.
  - Voltage where conductance stops
  - **Huge** manufacturing spread
- *k* is a constant
  - Depends on the physical size of the channel (length/width)
  - Depends on the manufacturing details



Ideal Performance vs. Reality





2N3958

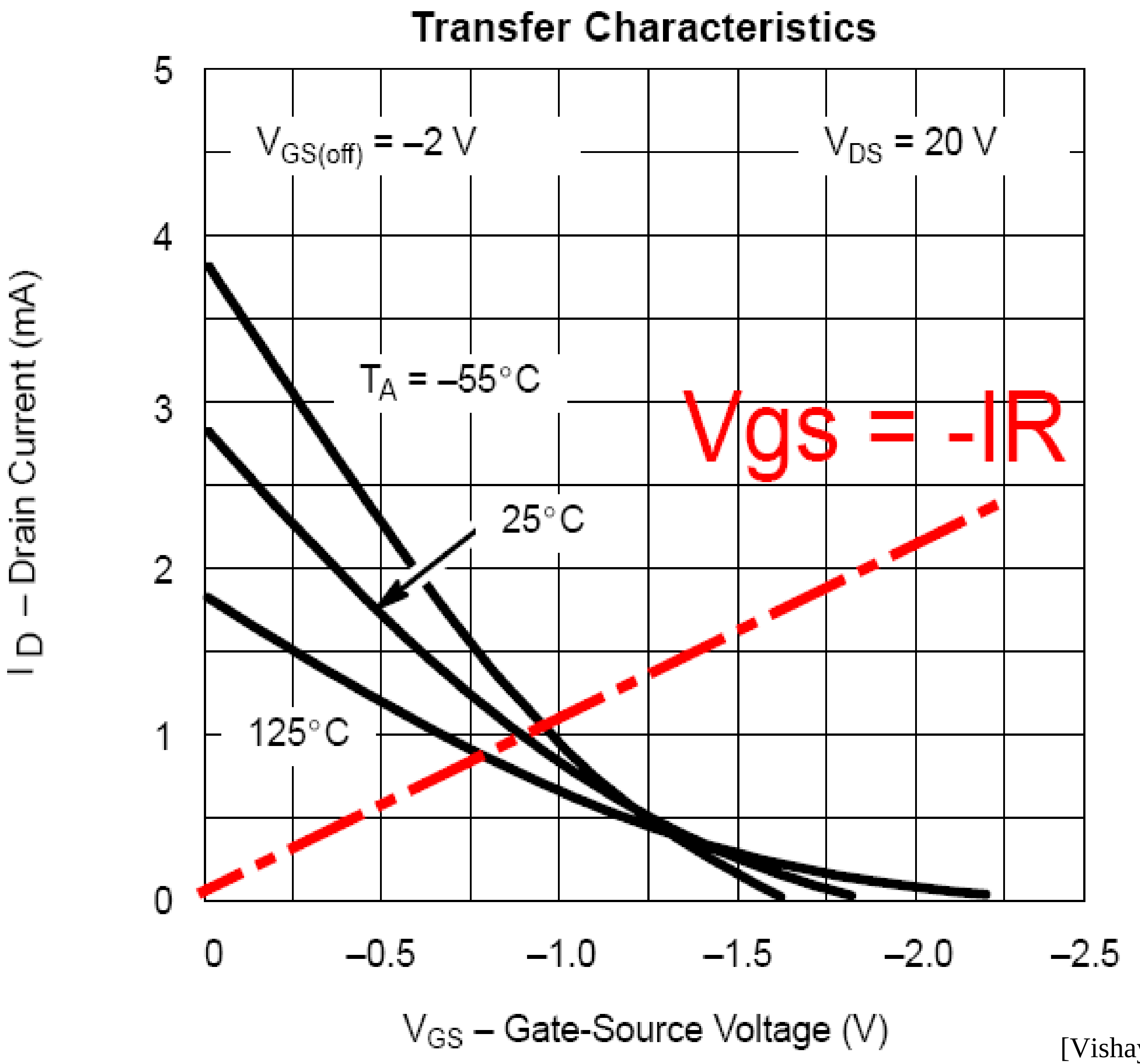
Vishay Siliconix

VISHAY

V_P

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
			Limits			
Parameter	Symbol	Test Conditions	Min	Typ[a]	Max	Unit
Static						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 µA, V_{DS} = 0 V	–50	–57		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 20 V, I_D = 1 nA	–1.0	–2	–4.5	
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	0.5	3	5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = –30 V, V_{DS} = 0 V		–10	–100	pA
		T_A = 150°C		–20	–500	nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 µA		–5	–50	pA
		T_A =125°C		–0.8	–250	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 µA	–0.5	–1.5	–4	
		I_D = 50 µA			–4.2	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V			2	
Dynamic						
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V f = 1 kHz	1	2.5	3	mS
Common-Source Output Conductance	g_{os}			2	35	µS

Solving for the current graphically



[Vishay 2N3958 datasheet]

Transconductance in the Saturation Region

- There is a quiescent current given by I_D.
- Use lower case symbols to represent small changes around the quiescent values
  - **Transconductance: $g_m = i_d/v_{gs}$**
    → Just the slope of I_D vs V_{GS} in the saturated region.
    → **Depends on I_D.**
  - Smaller variation for $V_{GS} < 0$ V.
  - Units: Ω^{-1}=mho (pronounced "Moe")
    → μmho or umho for 10^{-6} mho.
    → mmho for 10_{-3} mho.
    → Sometimes see ℧