Laboratory 7: Analog-to-digital and back again

This week we will learn how to use ADCs and DACs. We will convert an analog signal to a digital signal and then convert it back to an analog signal.

1. Analog-to-Digital

Use the ADC0820 to convert a constant voltage signal to a digital signal. Verify that the ADC is working the way you expect it to. What is the input voltage resolution of your ADC circuit?

2. Digital-to-Analog

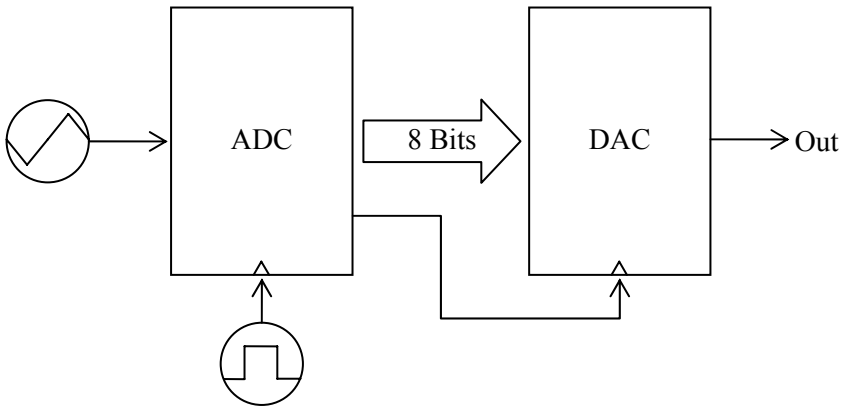
Use the TLC7524 to convert a digital signal provided by the slider switches on your breadboard to a constant analog signal. Verify that the DAC is working the way you expect it to. What is the output voltage resolution of your DAC circuit?

3. Analog-to-Digital and back again

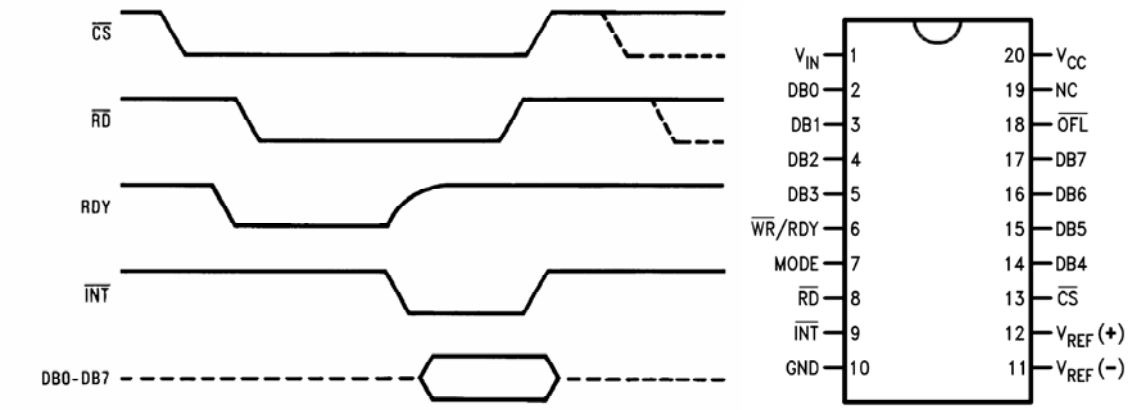
Attach the digital outputs of your ADC circuit to the digital inputs of the DAC circuit. Make sure that you connect the correct clocking outputs on the ADC to the DAC. Verify that the circuit performs the way you expect it to with constant input voltages, a sinusoid input, and a triangle wave input. Make sure that the sampling rate on the ADC is at least 10 times higher than the frequency of signals you are measuring. Compare the input analog signal to the output signal. Can you see the effects of digitization on the output signal?

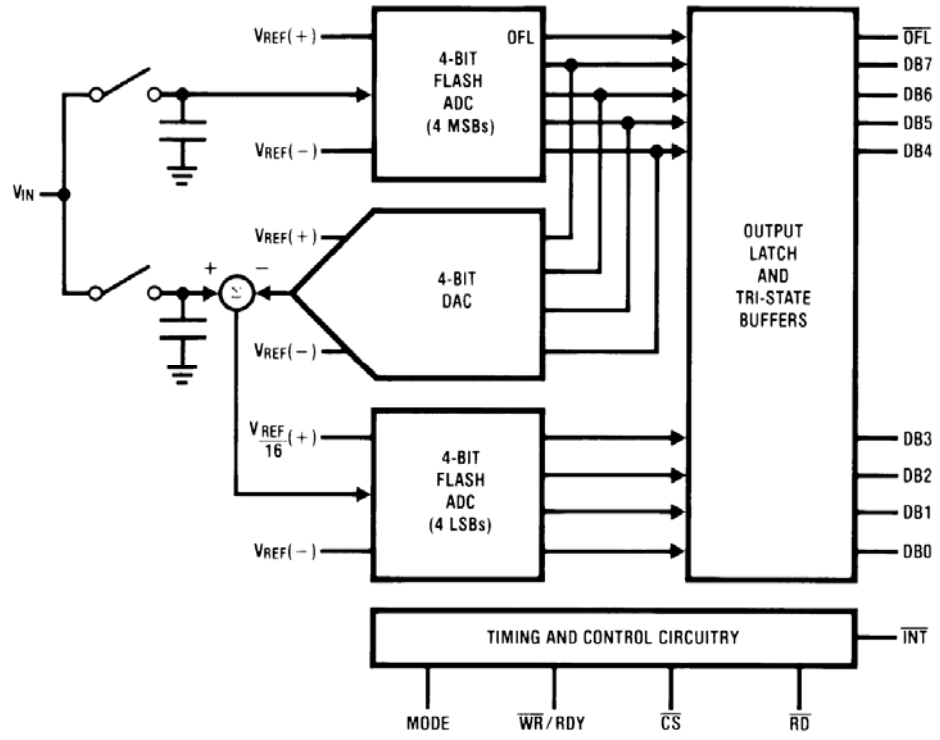
4. Aliasing

Reduce the sampling rate so that it is roughly 10 times smaller than the frequency of a sinewave input signal. What do you observe? Can you generate a similar effect with just a function generator connected to a digital oscilloscope?



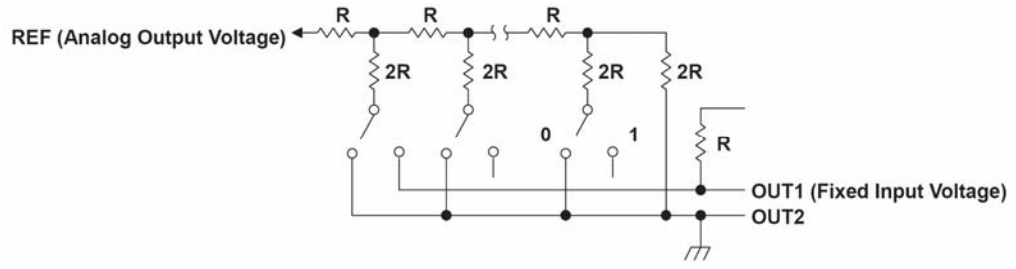
8-Bit ADC (ADC8020)



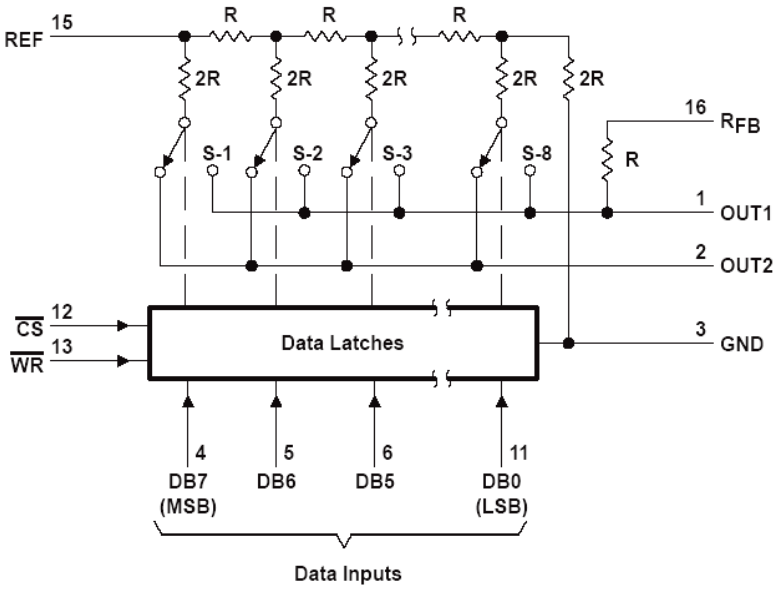


Pin	Name	Function
1	VIN	Analog input; range GND ≤ VIN ≤ VCC
2-5	DB0-DB3	TRI-STATE data outputs; bit 0 (LSB) to bit 3
6	WR/RDY	**WR-RD Mode** **WR**: With CS low, the conversion is started on the falling edge of WR. **RD Mode** **RDY**: RDY will go low after the falling edge of CS; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch.
7	MODE	Select mode: LOW = **RD** Mode HIGH = **WR-RD** Mode
8	RD	**WR-RD Mode** With CS low, the TRI-STATE data outputs (DB0-DB7) will be activated when RD goes low. **RD Mode** With CS low, the conversion will start with RD going LOW; also RD will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and INT going low indicates the completion of the conversion.
9	INT	INT going LOW indicates that the conversion is completed and the data result is in the output latch. INT is reset by raising edge on RD or CS.
10	GND	Ground
11	$V_{REF(-)}$	Bottom of resistor ladder; range: $GND \leq V_{REF(-)} \leq V_{REF(+)}$
12	$V_{REF(+)}$	Top of resistor ladder; range: $V_{REF(-)} \leq V_{REF(+)} \leq V_{CC}$
13	CS	CS must be low for the RD or WR to be recognized.
14-17	DB4-7	TRI-STATE data output—bits 4-7
18	OFL	Overflow—If the analog input is higher than the $V_{REF(+)}$, OFL will be LOW at the end of conversion. Can be used to cascade.
19	NC	No connection
20	V_{CC}	Power supply voltage

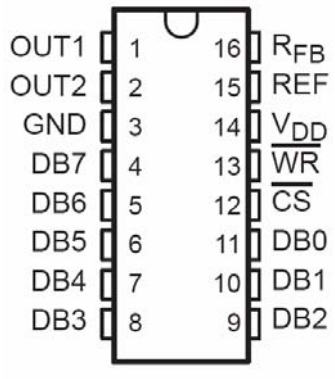
8-bit DAC (TLC7524)



Voltage Mode



Current mode



DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{ref}$ (255/256)
1 0 0 0 0 0 0 1	$-V_{ref}$ (129/256)
1 0 0 0 0 0 0 0	$-V_{ref}$ (128/256) = $-V_{ref}/2$
0 1 1 1 1 1 1 1	$-V_{ref}$ (127/256)
0 0 0 0 0 0 0 1	$-V_{ref}$ (1/256)
0 0 0 0 0 0 0 0	0

Current mode functional table