

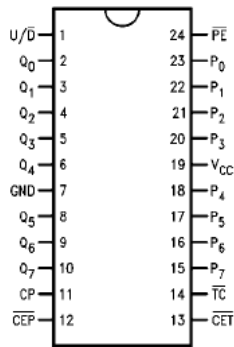
## Laboratory 7: Counters and State Machines

This week we learn how to use a counter, implement a state machine, and construct a microprocessor.

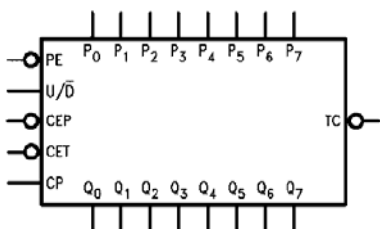
- Use a 74F269 as an eight-bit count-down counter. Its functional table, truth table, pinout, and logical symbol are shown below. Use your TTL pulse generator at a very low frequency as the clock input. Your counter should be designed to load a number from your slide switches when you push a button and then count down. Verify the truth table for  $\overline{TC}$ . What effects do  $\overline{CEP}$  and  $\overline{CET}$  have on  $\overline{TC}$ ? One can use  $\overline{TC}$  to control  $\overline{CEP}$  to ensure count-and-stop operation. What happens if you try to control  $\overline{CET}$  instead?
- Implement either Design Exercise 6-1 OR Design Exercise 6-2. You may construct the circuit with 74XXXXX-type chips OR use the FPGA on the DE2 board (your Quartus II project can be in either schematic or Verilog format).

**Alternate exercise for 2:** Construct a Nios II embedded microprocessor in Verilog and load onto the DE2 FPGA. The microprocessor should have an 8-bit input register, an 8-bit output register, a CPU reset input, and a 50 MHz clock input. Load the C program *lights.c* and test that the switches control the respective LEDs on the DE2. Measure the propagation delay between the input and output registers and compare to what you would expect from an FPGA without the microprocessor. Estimate the number of clock cycles for the CPU to convert 1-bit.

### 74F269 counter: basic operation tables



Pin Names	Description
P <sub>0</sub> -P <sub>7</sub>	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
U/ $\overline{D}$	Up-Down Count Control Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$\overline{CET}$	Count Enable Trickle Input (Active LOW)
CP	Clock Input
$\overline{TC}$	Terminal Count Output (Active LOW)
Q <sub>0</sub> -Q <sub>7</sub>	Flip-Flop Outputs



$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/ $\overline{D}$	CP	Function
L	X	X	X	↗	Parallel Load All Flip-Flops
H	H	X	X	↗	Hold
H	X	H	X	↗	Hold ( $\overline{TC}$ Held HIGH)
H	L	L	H	↗	Count Up
H	L	L	L	↗	Count Down

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = Transition LOW-to-HIGH

