DSP Project Purchases

- Budget = $200.00 USD per team.

- All purchases will go through the instructor to Sylvia Stout.

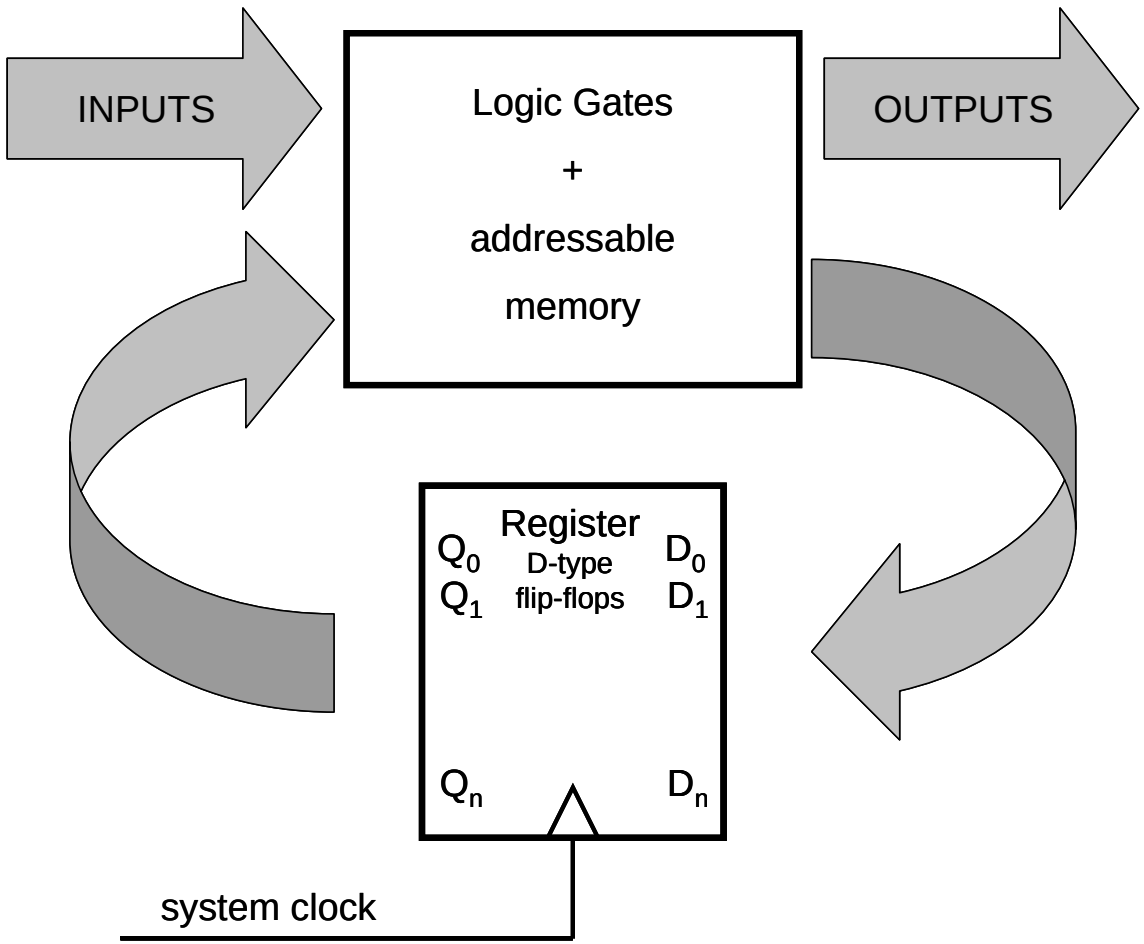
- You must provide an internet shopping cart printout with all the part numbers. An electronic version is useful and will help speed up the purchase.

- If you buy a part at a local store, then you must keep the receipt and submit it to the instructor at the end of the course.

- You are encouraged to use the parts in the lab to perfect your design, however your final device should include only new non-lab parts (except wire).

State Machine

Definition: A machine that makes predictable transitions through a sequence of states, based on external inputs and the current state of the machine.

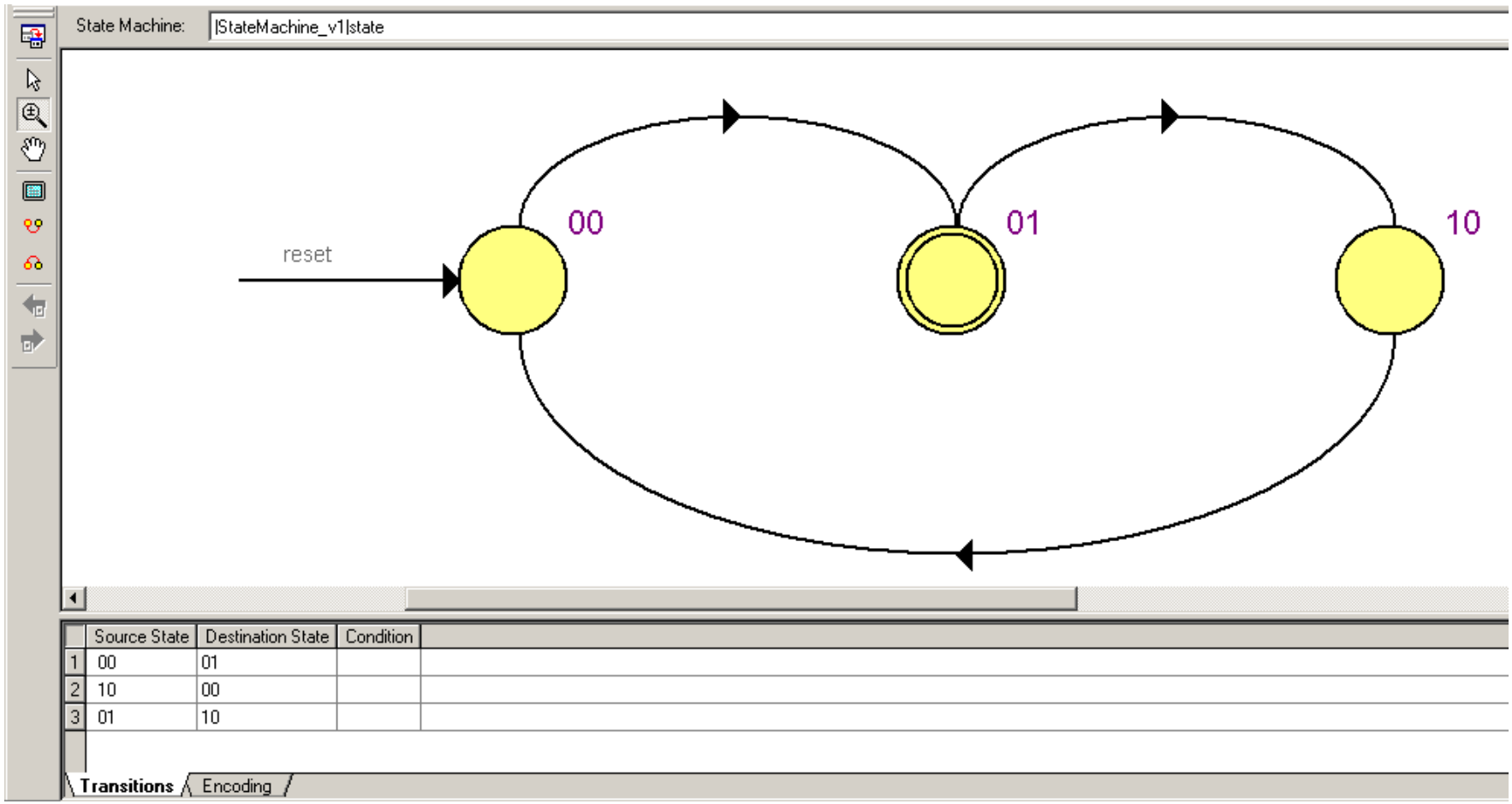


State Machines in Verilog

```
1  // Verilog state machine implementation of the divide-by-3 counter
2  module StateMachine_v1(clk, reset, out);
3      input clk, reset;        // clock and reset declarations
4      output reg out;          // output register declaration
5
6      reg [1:0] state;         // this register holds the state of the machine
7
8      always @(state)          // This always block indicates how the output
9          begin                // should relate to the machine state
10         case (state)
11             2'b00: out = 1'b0;
12             2'b01: out = 1'b1;
13             2'b10: out = 1'b0;
14 //          2'b11: out = 1'b0;      // only required for completeness (not necessary)
15 //          default: out = 1'b0;    // default statement guarantees completeness (not necessary)
16         endcase
17         end
18
19     always @(posedge clk or posedge reset)  // This always block  constructs the
20         begin                               // sequence table
21         if (reset==1) state = 2'b00;
22         else
23         case (state)
24             2'b00: state = 2'b01;
25             2'b01: state = 2'b10;
26             2'b10: state = 2'b00;
27 //          2'b11: state = 2'b00;   // only required for completeness (not necessary)
28 //          default: state = 2'b00; // default statement guarantees completeness (not necessary)
29         endcase
30         end
31 endmodule
32
```

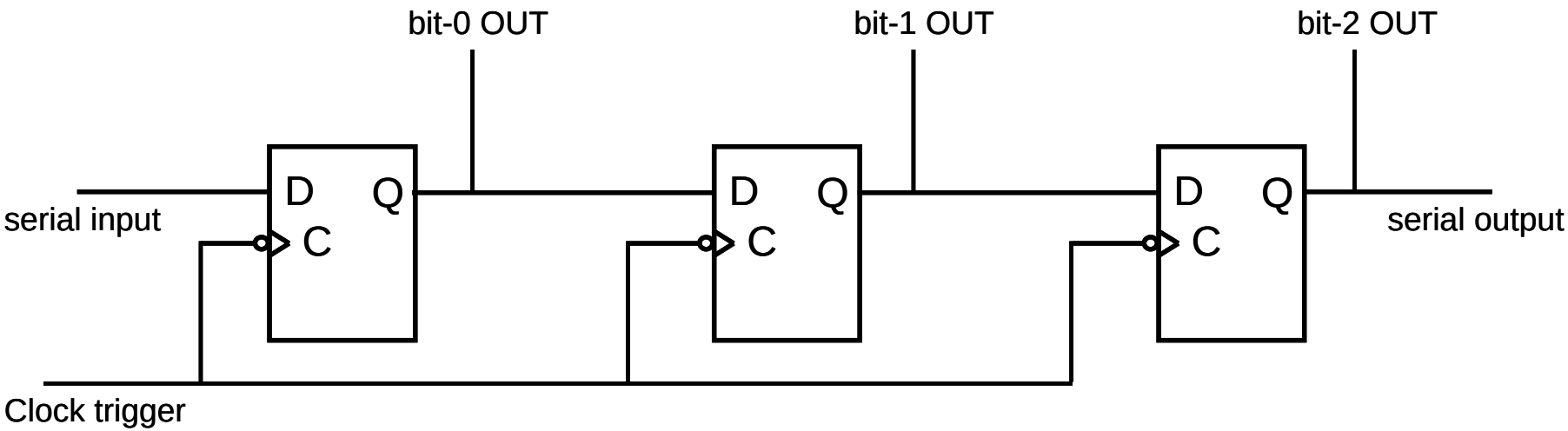
State Machines in Quartus II

Tools > Netlist Viewers > State Machine Viewer



Note: The Quartus II compiler will only find the State Machine if you follow the Verilog example code fairly closely.

Shift Register Circuit



Shift Register in Verilog

```
1  module ShiftRegister(serial_input, clock, reset, output_register, serial_output);
2      input serial_input;                  // serial input line of the shift register
3      input clock;                         // clock input line of the shift register
4      input reset;                         // reset line for resetting the shift register to ZERO
5      output reg [7:0] output_register;    // Register for the shift register
6      output serial_output;              // serial output line (equivalent to output_register[7])
7      initial
8          begin
9          output_register = 8'b00000000;  // Start with an empty shift register
10         end
11
12     // connect the serial output line to the bit 8 of the shift register
13     assign serial_output = output_register[7];
14
15     always @ (posedge clock or posedge reset)
16         begin
17         if (reset == 1)
18             begin
19             output_register <= 8'b00000000;     // reset the shift register to ZERO
20             end
21         else
22             begin
23
24             // shifts all the shift register bits to the next bit
25             output_register <= output_register << 1;
26
27             // loads the serial input into the first shift register bit
28             output_register[0] <= serial_input;
29             end
30         end
31
32 endmodule
```

Shift Register in Verilog

```
1  module ShiftRegister(serial_input, clock, reset, output_register, serial_output);
2      input serial_input;                  // serial input line of the shift register
3      input clock;                         // clock input line of the shift register
4      input reset;                         // reset line for resetting the shift register to ZERO
5      output reg [7:0] output_register;    // Register for the shift register
6      output serial_output;              // serial output line (equivalent to output_register[7])
7      initial
8          begin
9          output_register = 8'b00000000;  // Start with an empty shift register
10         end
11
12     // connect the serial output line to the bit 8 of the shift register
13     assign serial_output = output_register[7];
14
15     always @ (posedge clock or posedge reset)
16         begin
17         if (reset == 1)
18             begin
19             output_register <= 8'b00000000;     // reset the shift register to ZERO
20             end
21         else
22             begin
23
24             // shifts all the shift register bits to the next bit
25             output_register <= output_register << 1;
26
27             // loads the serial input into the first shift register bit
28             output_register[0] <= serial_input;
29             end
30         end
31
32 endmodule
```

use the left bit shift operator <<

Microprocessors

Microprocessors are a generalization of a state machines which fit on a single IC. They have the following components:

[image from jkslade.net]

- **Instruction set:** These are the basic instructions that the CPU can perform (add, multiply, store memory, retrieve memory, etc …)

- **Memory:** this is generally a 2-d array of shift registers (FIFO) where a program (i.e. a series of instructions) and the bits that it manipulates are stored. Exact memory architecture varies.

  → Memory for program

  → Memory for bits

  → Attached peripherals (input/output) are treated as memory locations.

Microprocessors perform 1 instruction at a time. A single instruction can take mutiple clock cycles. All operations are performed in a sequential manner.

Microprocessor (vs. FPGAs)

Advantages:

- Conceptually simple sequential operation.
- Easy to program (i.e. C, Basic, Java, Fortran …).
- Enormous number of function libraries to use.
- It's a computer minus screen, keyboard, and mouse.

[image from jkslade.net]

Disadvantages:

- Slow (multiple clock cycles per instruction).
- Non-parallel … only sequential.
- Operating systems can be unreliable.
- Non-deterministic timing operation (interrupts …).

Nios II microprocessor

You can program a microprocessor(s) onto an FPGA.

The Altera soft-processor is called Nios II and is programmed onto the FPGA using the SOPC builder (SOPC = System On a Programmable Chip).

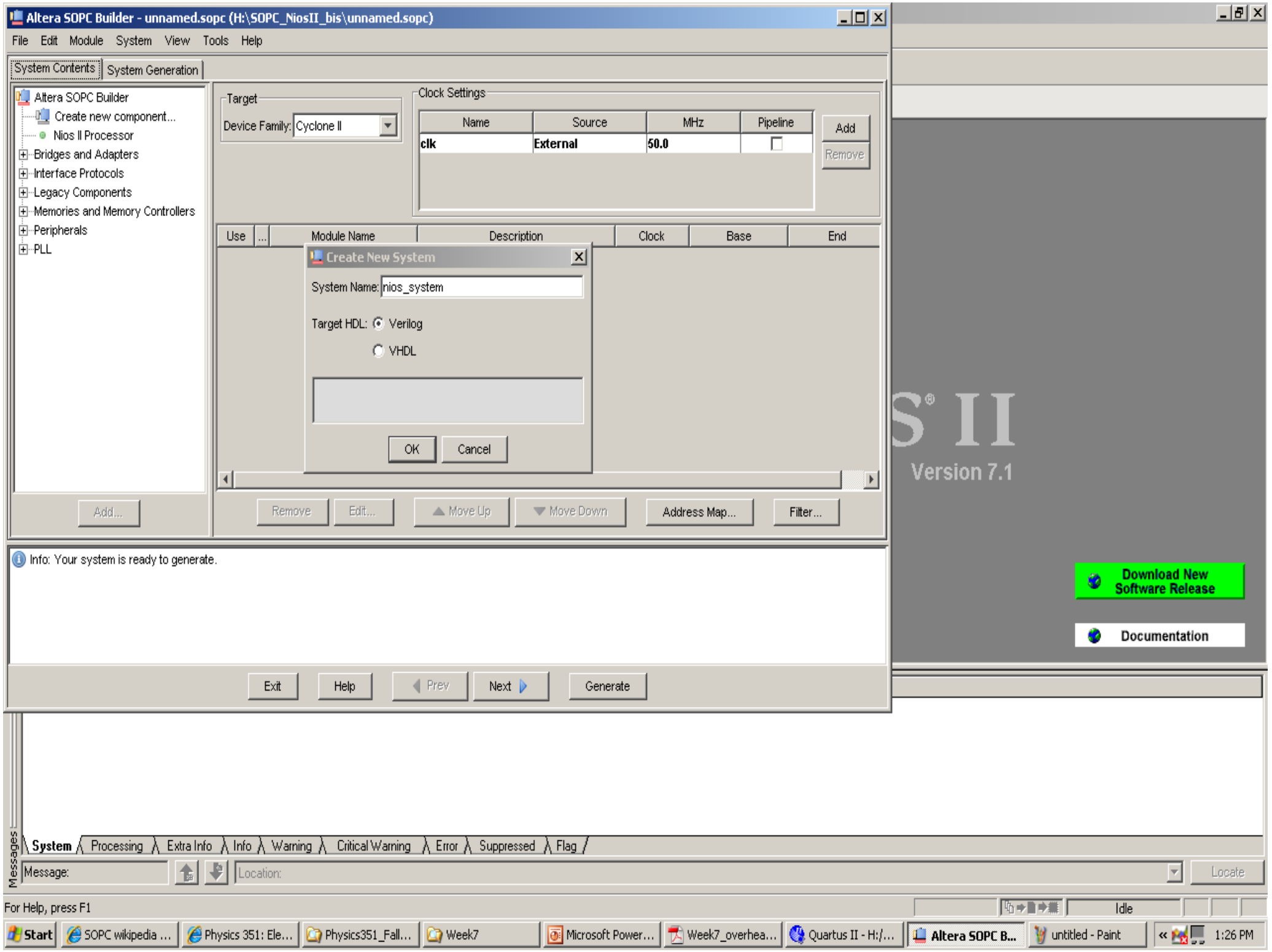
I found that Nios II was not well supported by the Quartus II Web Edition (v7.1)

→ Use the Quartus II full subscription version

(Electronics lab, Morton 240, Swem 134)

The SOPC builder can be found in Quartus II at

Tools > SOPC Builder …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File Edit Module System View Tools Help
System Contents
System Generation
Altera SOPC Builder
Create new component...
Nios II Processor
Bridges and Adapters
Interface Protocols
Legacy Components
Memories and Memory Controllers
Peripherals
PLL
Add...
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Device Family: Cyclone II
Clock Settings
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MHz
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Remove
Use
Module Name
Description
Clock
Base
End
Create New System
System Name: nios_system
Target HDL: Verilog
VHDL
OK
Cancel
Remove
Edit...
Move Up
Move Down
Address Map...
Filter...
Info: Your system is ready to generate.
Exit
Help
Prev
Next
Generate
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Version 7.1
Download New Software Release
Documentation
Messages
System
Processing
Extra Info
Info
Warning
Critical Warning
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Message:
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Locate
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Idle
Start
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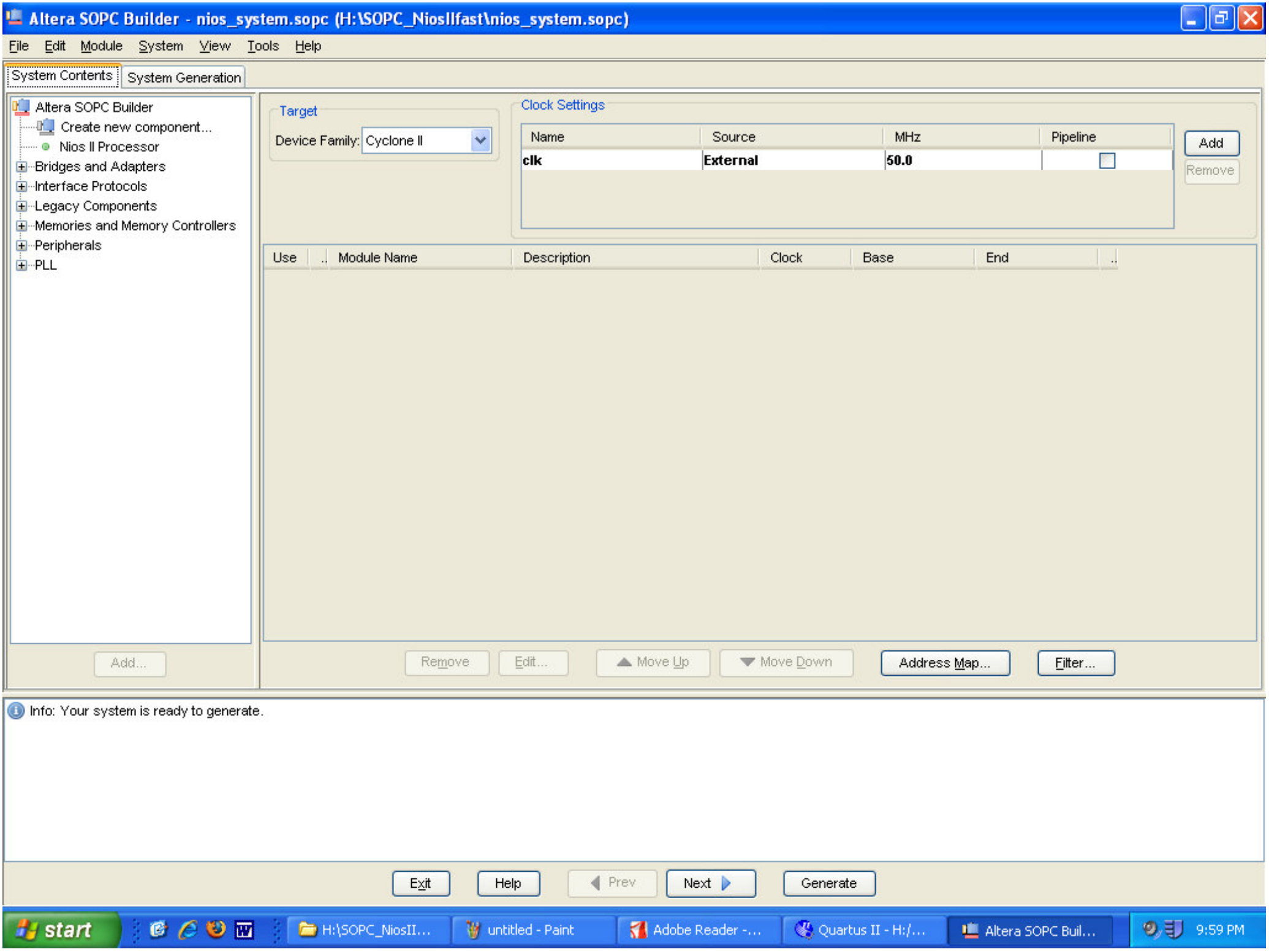
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File Edit Module System View Tools Help
System Contents
System Generation
Altera SOPC Builder
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Nios II Processor
Bridges and Adapters
Interface Protocols
Legacy Components
Memories and Memory Controllers
Peripherals
PLL
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Device Family: Cyclone II
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Module Name
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Clock
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End
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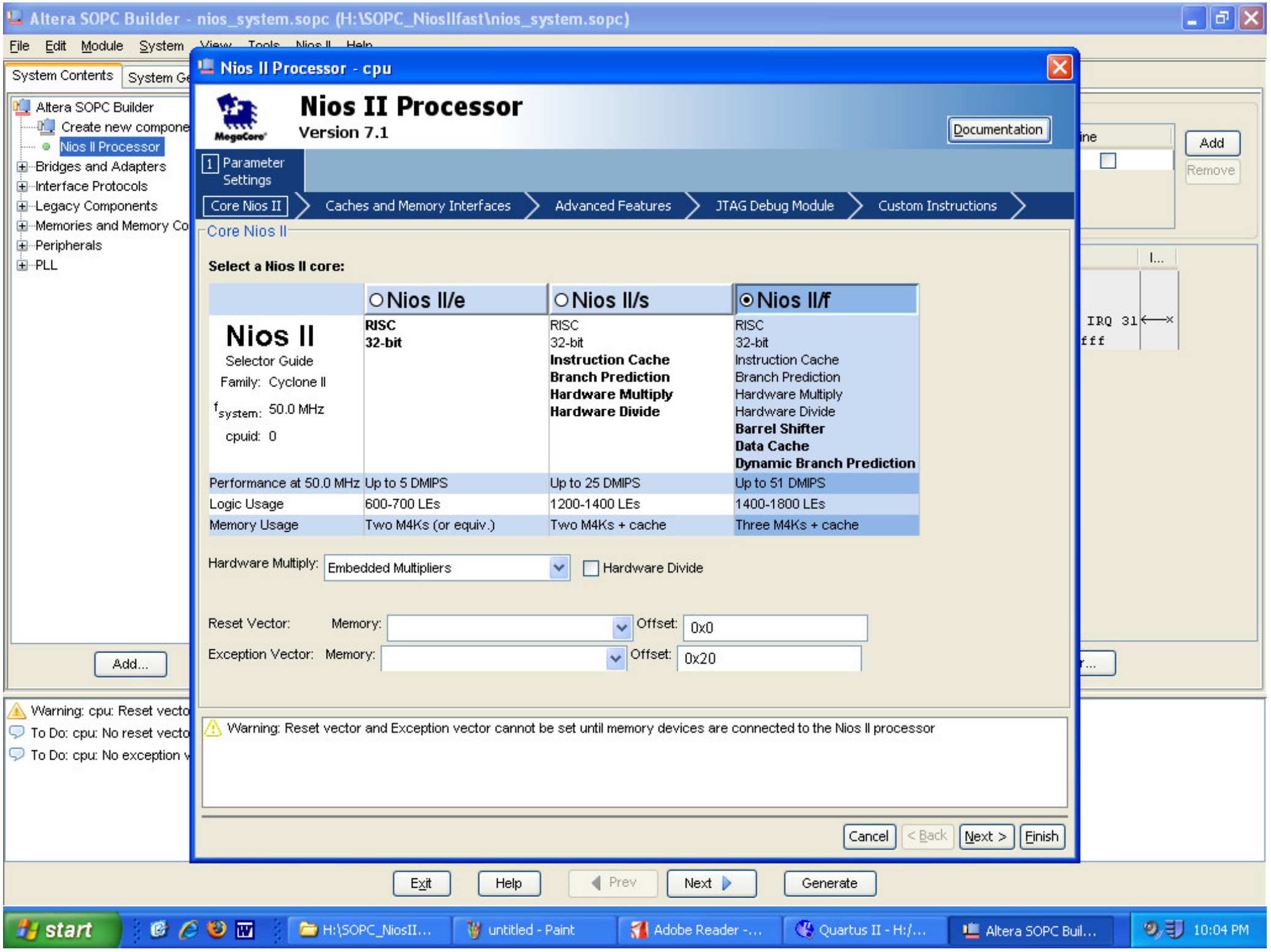
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Interface Protocols
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Memories and Memory Co
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Nios II Processor - cpu
Nios II Processor
Version 7.1
Documentation
1 Parameter Settings
Core Nios II
Caches and Memory Interfaces
Advanced Features
JTAG Debug Module
Custom Instructions
Core Nios II
Select a Nios II core:
Nios II
Selector Guide
Family: Cyclone II
f system: 50.0 MHz
cpuid: 0
Nios II/e
RISC
32-bit
Nios II/s
RISC
32-bit
Instruction Cache
Branch Prediction
Hardware Multiply
Hardware Divide
Nios II/f
RISC
32-bit
Instruction Cache
Branch Prediction
Hardware Multiply
Hardware Divide
Barrel Shifter
Data Cache
Dynamic Branch Prediction
Performance at 50.0 MHz
Up to 5 DMIPS
Up to 25 DMIPS
Up to 51 DMIPS
Logic Usage
600-700 LEs
1200-1400 LEs
1400-1800 LEs
Memory Usage
Two M4Ks (or equiv.)
Two M4Ks + cache
Three M4Ks + cache
Hardware Multiply: Embedded Multipliers
Hardware Divide
Reset Vector: Memory: Offset: 0x0
Exception Vector: Memory: Offset: 0x20
Warning: Reset vector and Exception vector cannot be set until memory devices are connected to the Nios II processor
Cancel
< Back
Next >
Finish
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Remove
IRQ 31
Warning: cpu: Reset vecto
To Do: cpu: No reset vecto
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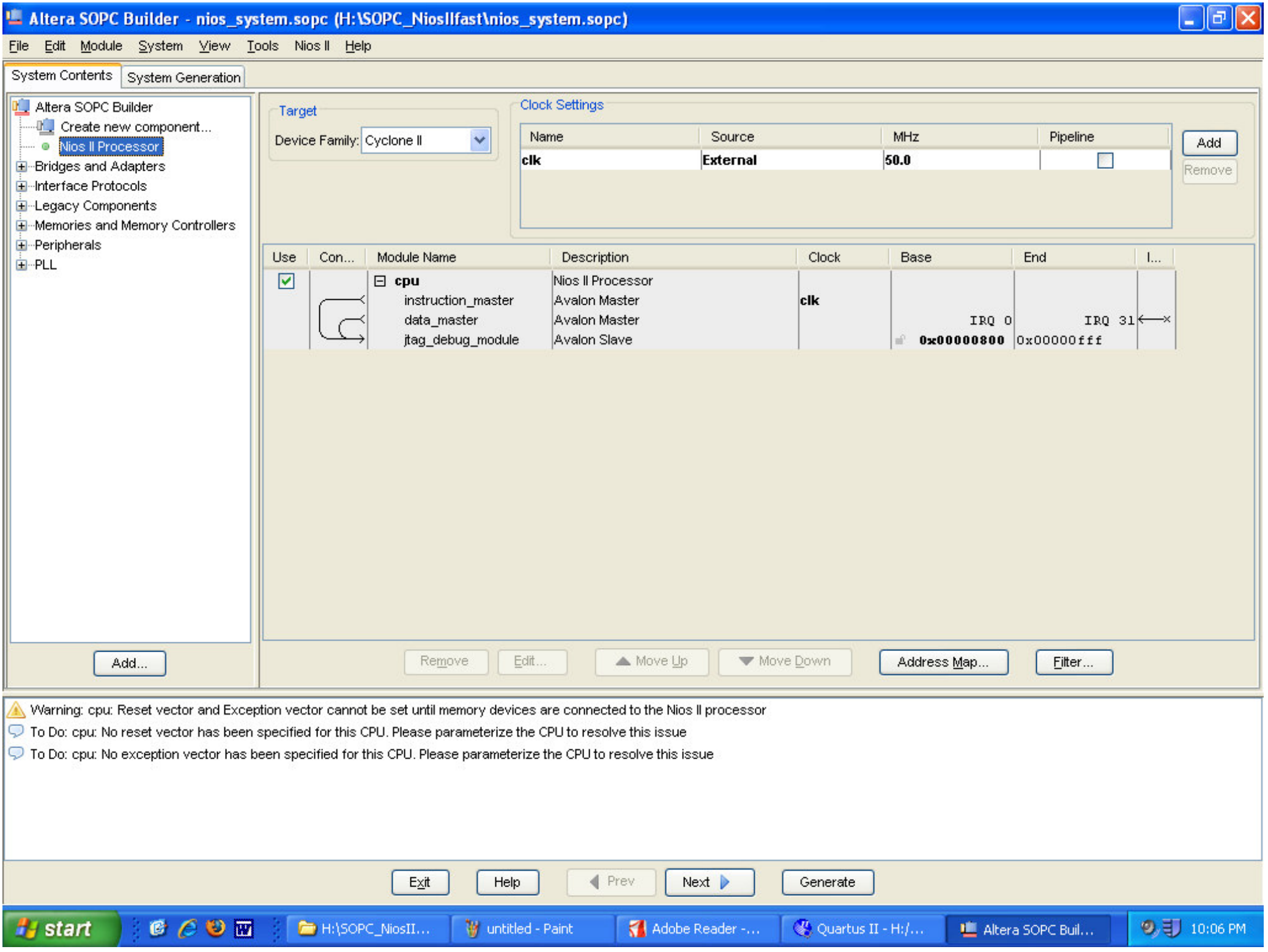
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Legacy Components
Memories and Memory Controllers
Peripherals
PLL
Add...
Target
Device Family: Cyclone II
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Module Name
Description
Clock
Base
End
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instruction_master
Avalon Master
clk
data_master
Avalon Master
IRQ 0
IRQ 31
jtag_debug_module
Avalon Slave
0x00000800
0x00000fff
Remove
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Move Up
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Address Map...
Filter...
Warning: cpu: Reset vector and Exception vector cannot be set until memory devices are connected to the Nios II processor
To Do: cpu: No reset vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
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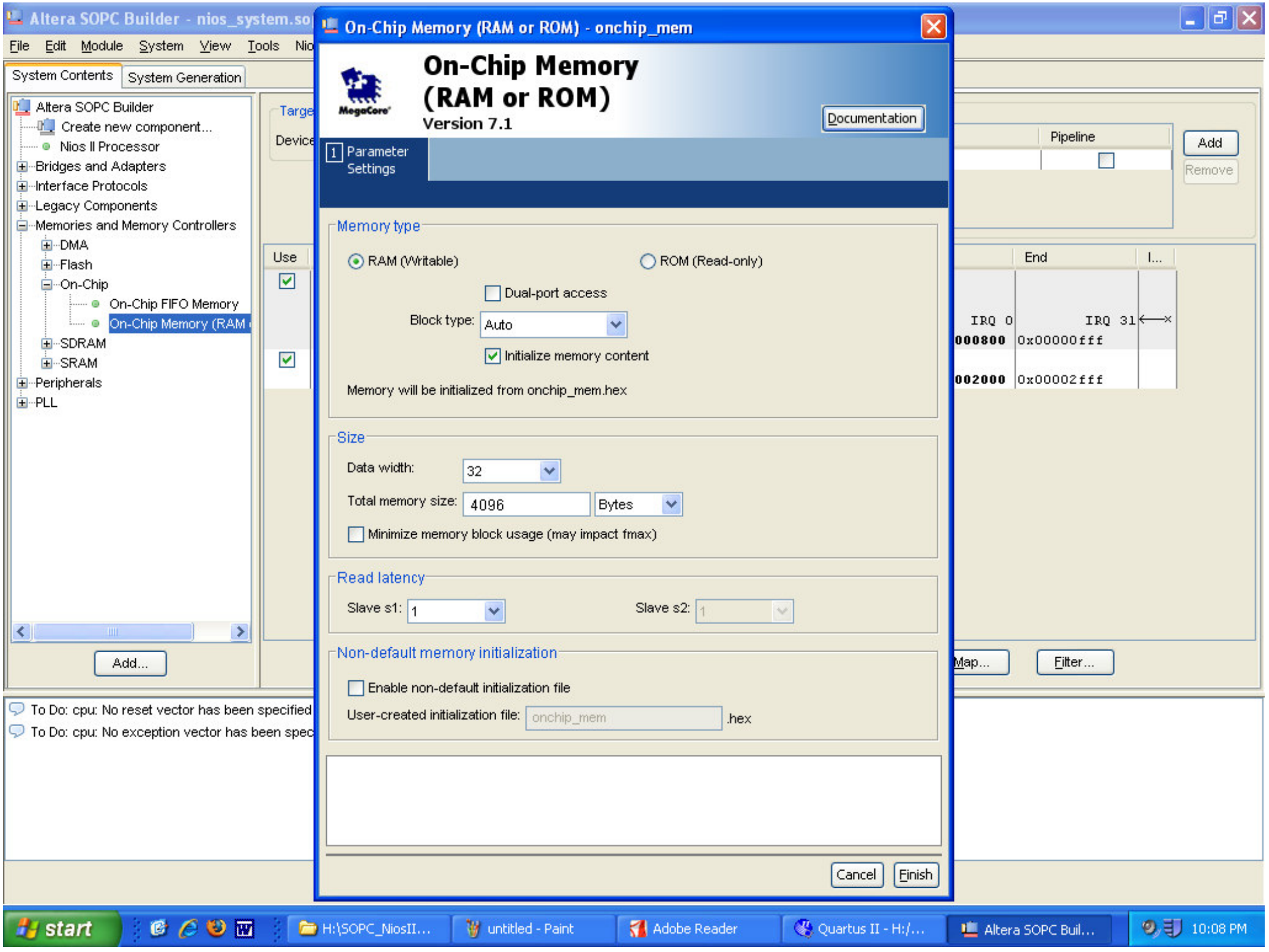
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Altera SOPC Builder
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Bridges and Adapters
Interface Protocols
Legacy Components
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To Do: cpu: No exception vector has been spec
On-Chip Memory (RAM or ROM) - onchip_mem
On-Chip Memory (RAM or ROM)
Version 7.1
Documentation
1 Parameter Settings
Memory type
RAM (Writable)
ROM (Read-only)
Dual-port access
Block type: Auto
Initialize memory content
Memory will be initialized from onchip_mem.hex
Size
Data width: 32
Total memory size: 4096 Bytes
Minimize memory block usage (may impact fmax)
Read latency
Slave s1: 1
Slave s2: 1
Non-default memory initialization
Enable non-default initialization file
User-created initialization file: onchip_mem .hex
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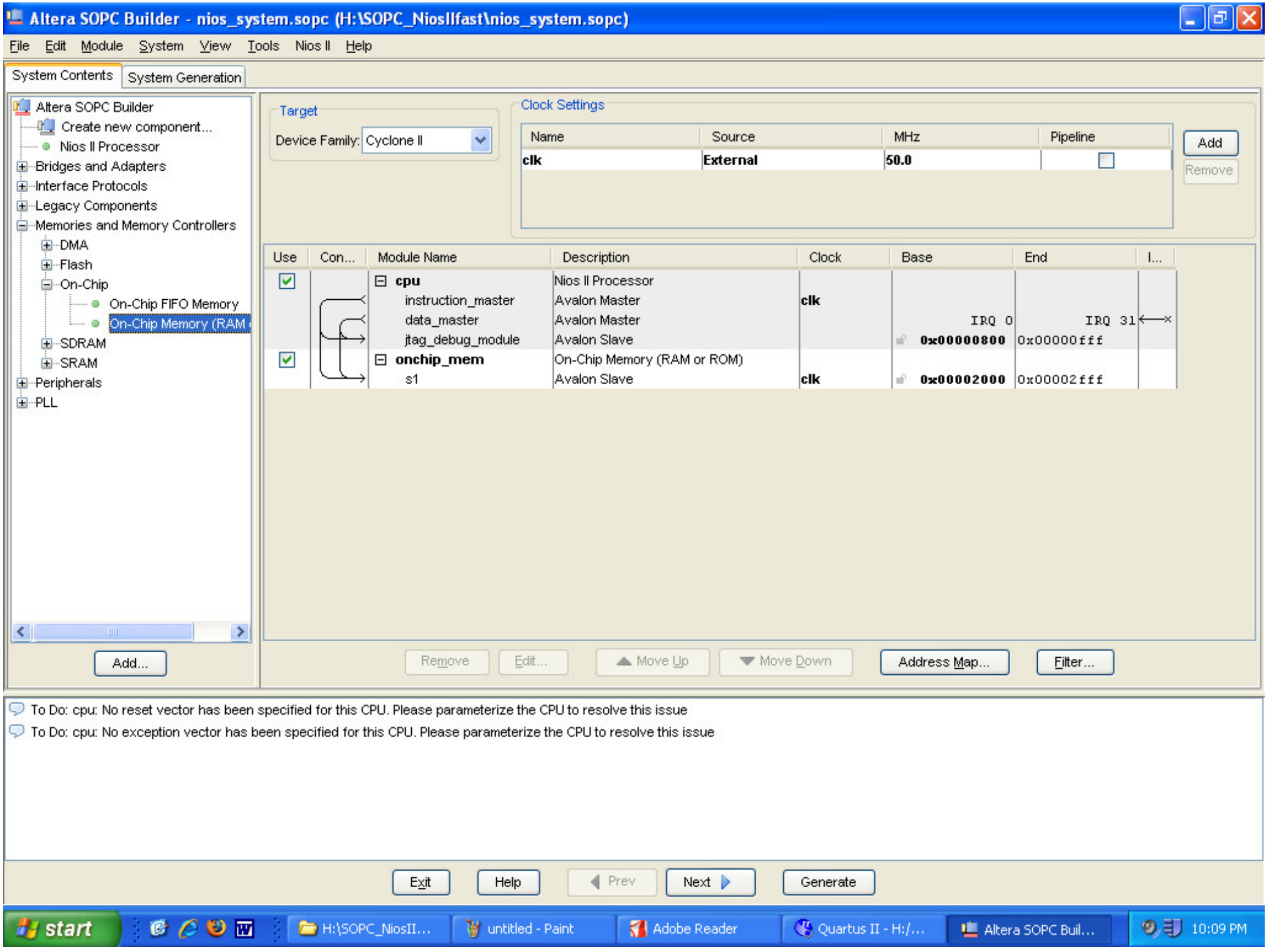
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Memories and Memory Controllers
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instruction_master
Avalon Master
clk
data_master
Avalon Master
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jtag_debug_module
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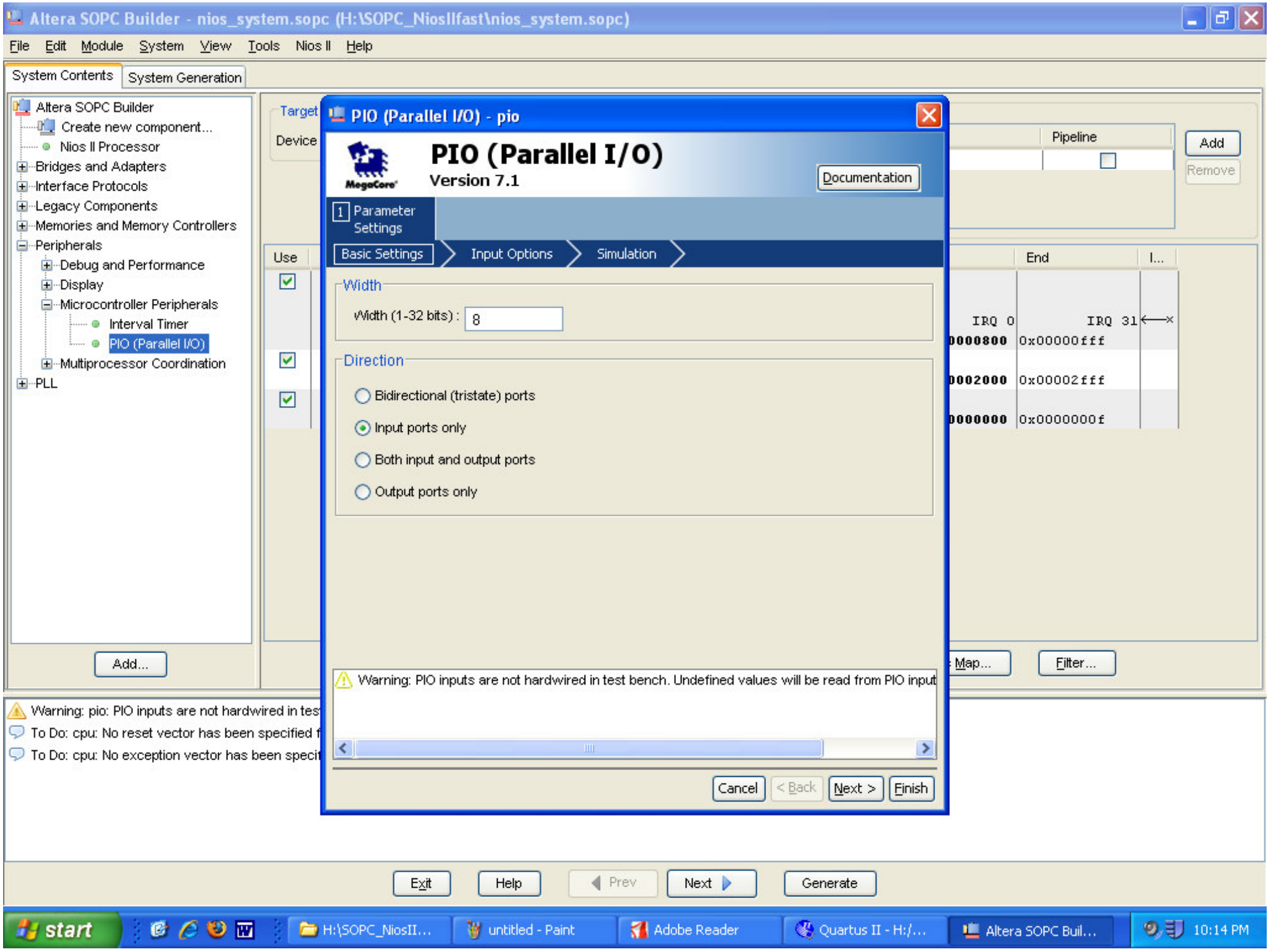
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Microcontroller Peripherals
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PIO (Parallel I/O)
Version 7.1
MegaCore
Documentation
1 Parameter Settings
Basic Settings
Input Options
Simulation
Width
Width (1-32 bits) : 8
Direction
Bidirectional (tristate) ports
Input ports only
Both input and output ports
Output ports only
Warning: PIO inputs are not hardwired in test bench. Undefined values will be read from PIO input
Cancel
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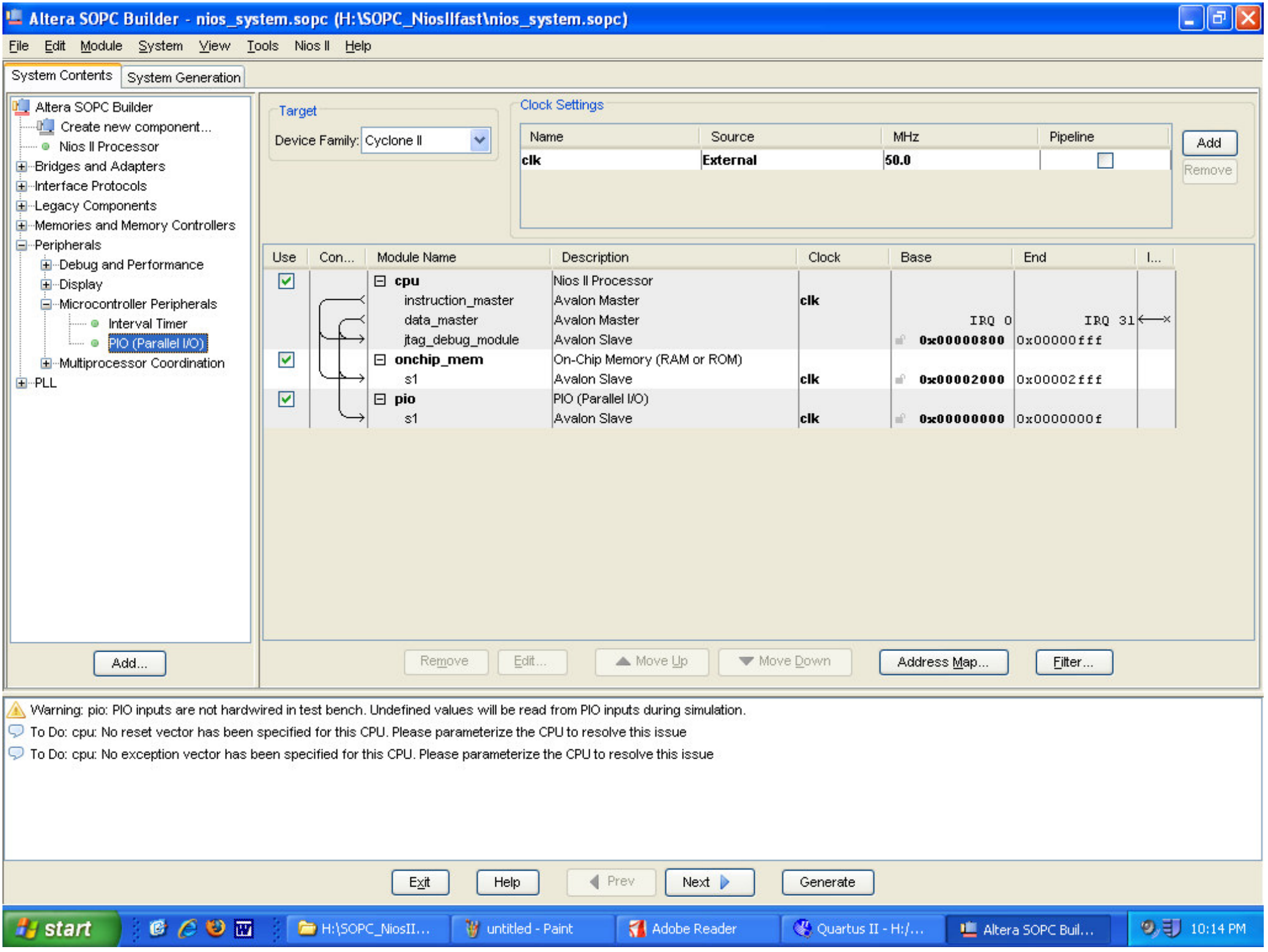
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Display
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PIO (Parallel I/O)
Multiprocessor Coordination
PLL
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clk
data_master
Avalon Master
IRQ 0
IRQ 31
jtag_debug_module
Avalon Slave
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0x00000fff
onchip_mem
On-Chip Memory (RAM or ROM)
s1
Avalon Slave
clk
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To Do: cpu: No reset vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
To Do: cpu: No exception vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
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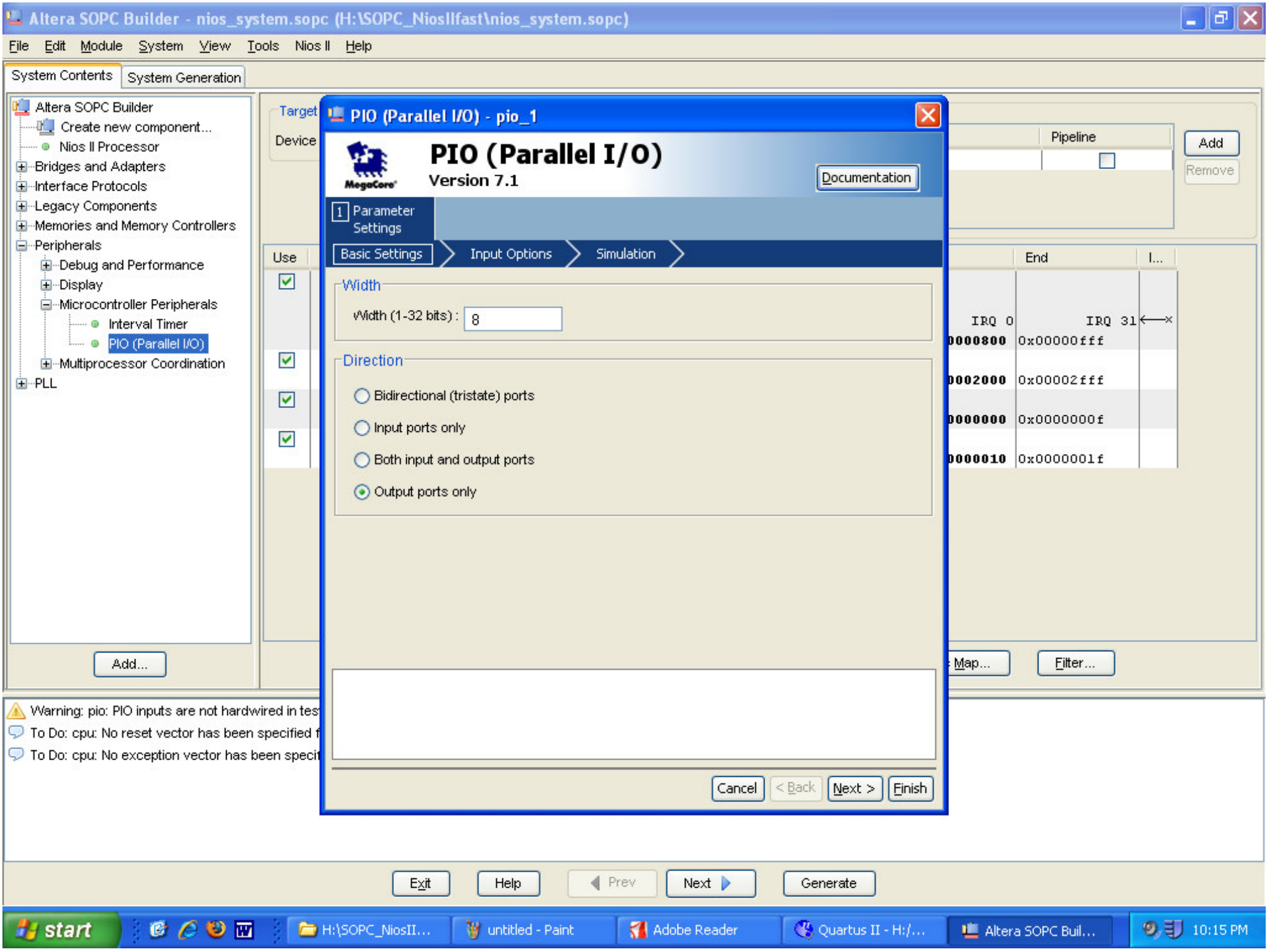
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PLL
Add...
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Add
Remove
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IRQ 0
IRQ 31
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0x00002fff
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Map...
Filter...
PIO (Parallel I/O) - pio_1
PIO (Parallel I/O)
Version 7.1
Documentation
1 Parameter Settings
Basic Settings
Input Options
Simulation
Width
Width (1-32 bits) : 8
Direction
Bidirectional (tristate) ports
Input ports only
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Output ports only
Cancel
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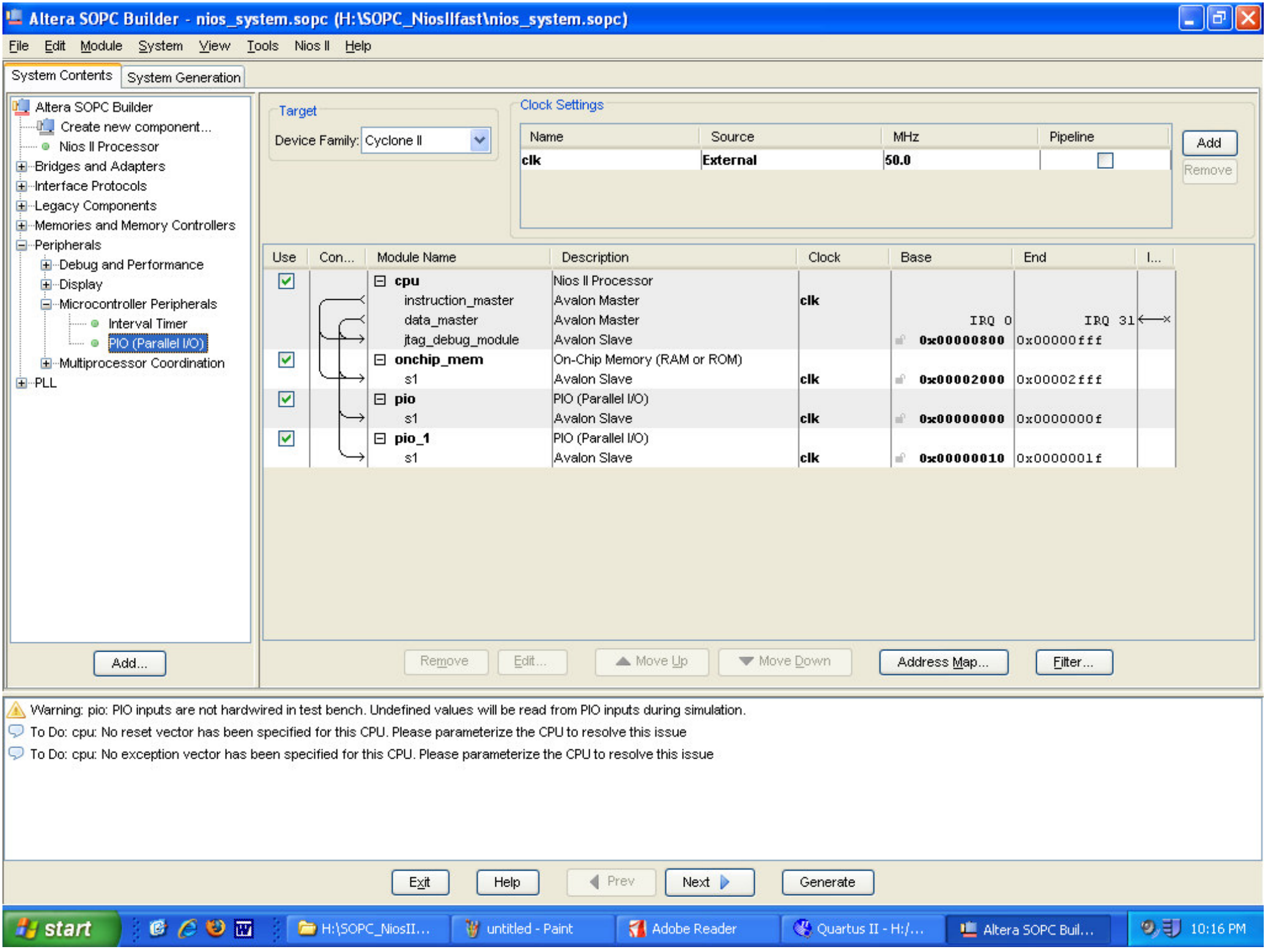
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Peripherals
Debug and Performance
Display
Microcontroller Peripherals
Interval Timer
PIO (Parallel I/O)
Multiprocessor Coordination
PLL
Add...
Target
Device Family: Cyclone II
Clock Settings
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Module Name
Description
Clock
Base
End
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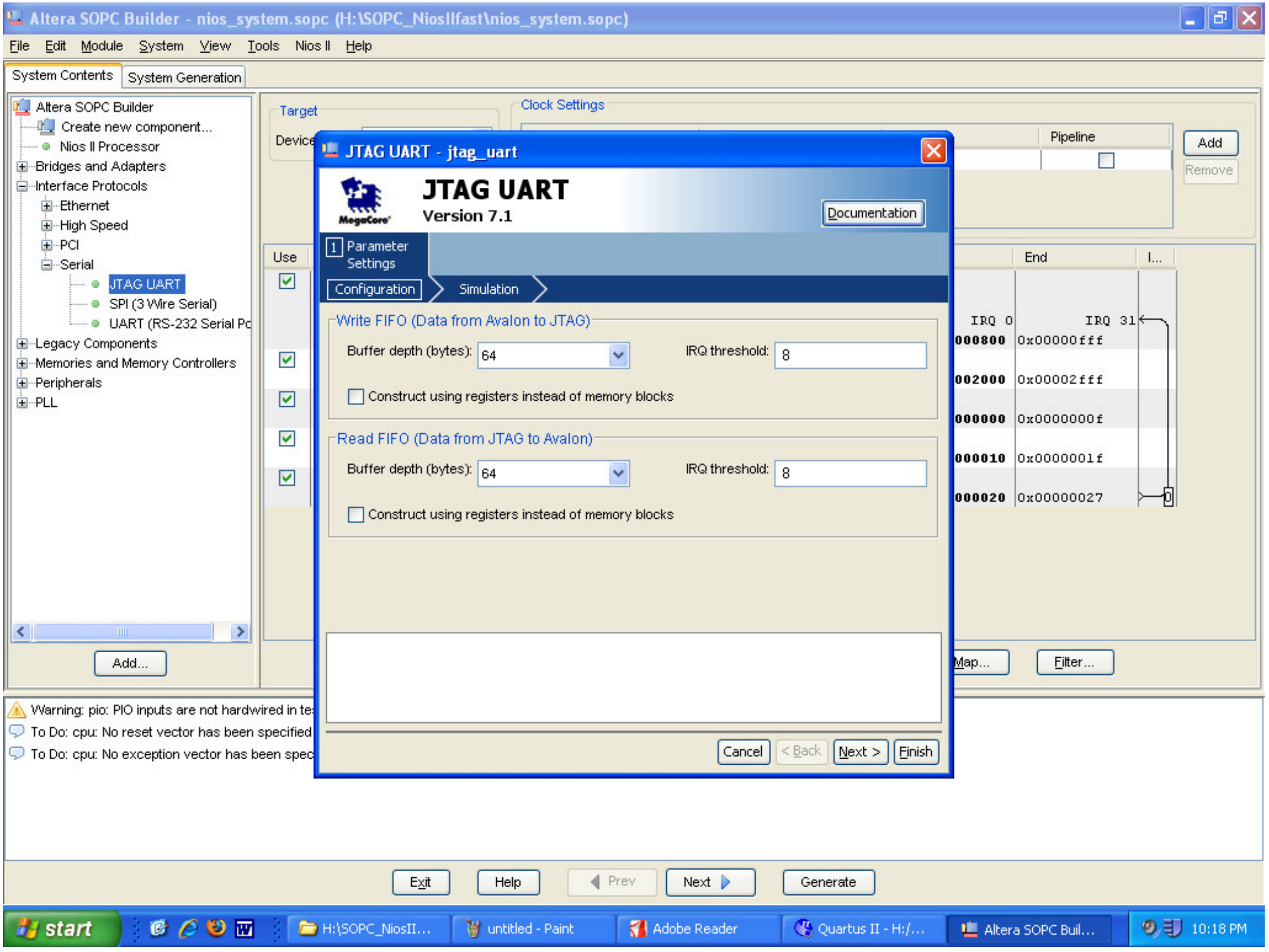
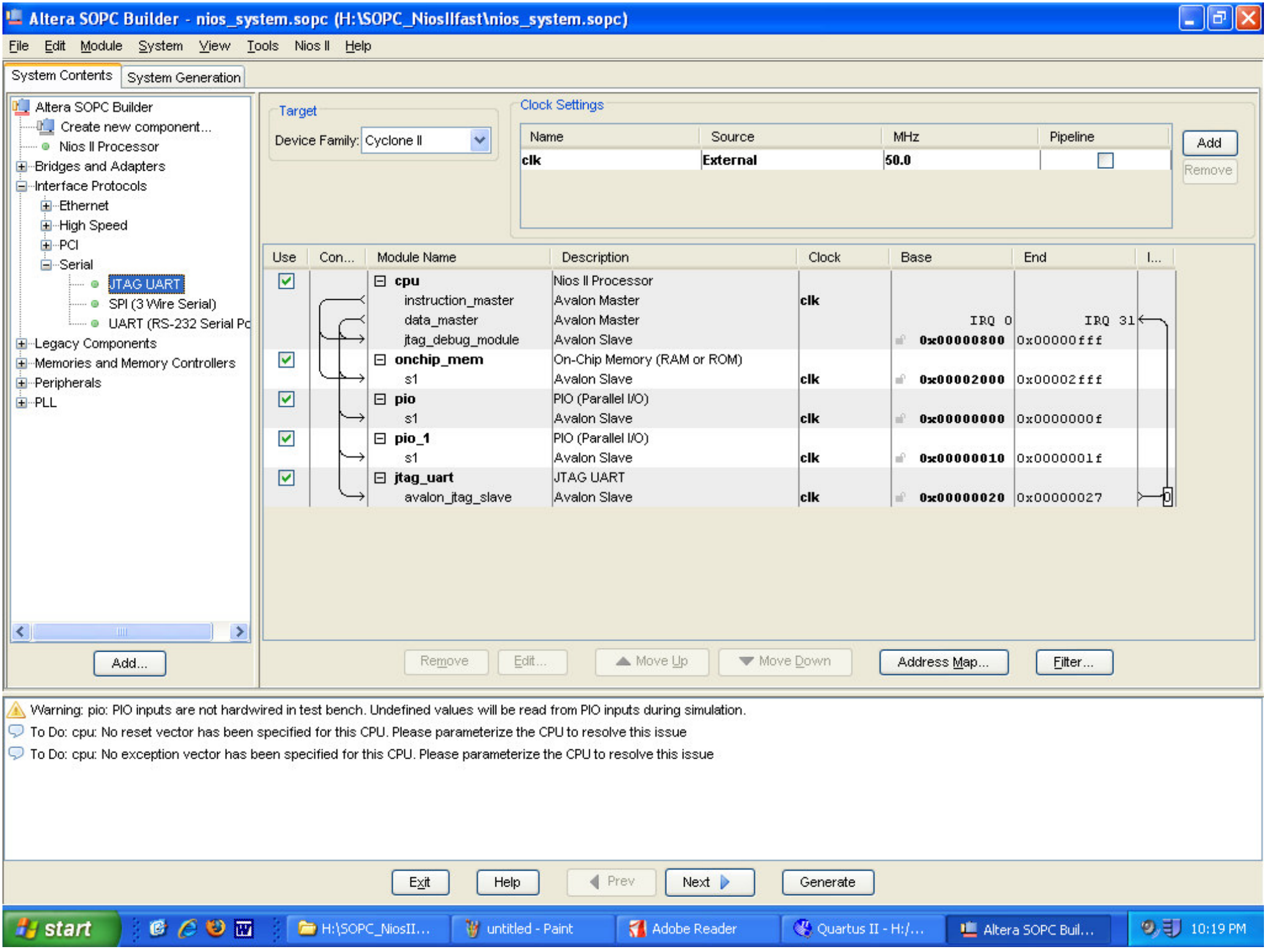
cpu
Nios II Processor
instruction_master
Avalon Master
clk
data_master
Avalon Master
IRQ 0
IRQ 31
jtag_debug_module
Avalon Slave
0x00000800
0x00000fff
onchip_mem
On-Chip Memory (RAM or ROM)
s1
Avalon Slave
clk
0x00002000
0x00002fff
pio
PIO (Parallel I/O)
s1
Avalon Slave
clk
0x00000000
0x0000000f
pio_1
PIO (Parallel I/O)
s1
Avalon Slave
clk
0x00000010
0x0000001f
Remove
Edit...
Move Up
Move Down
Address Map...
Filter...
Warning: pio: PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.
To Do: cpu: No reset vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
To Do: cpu: No exception vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
Exit
Help
Prev
Next
Generate
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera SOPC Buil...
10:16 PM


Altera SOPC Builder - nios_system.sopc (H:\SOPC_NiosIIfast\nios_system.sopc)
File Edit Module System View Tools Nios II Help
System Contents
System Generation
Altera SOPC Builder
Create new component...
Nios II Processor
Bridges and Adapters
Interface Protocols
Ethernet
High Speed
PCI
Serial
JTAG UART
SPI (3 Wire Serial)
UART (RS-232 Serial Pc
Legacy Components
Memories and Memory Controllers
Peripherals
PLL
Add...
Target
Clock Settings
Pipeline
Add
Remove
Use
End
IRQ 0
IRQ 31
000800 0x00000fff
002000 0x00002fff
000000 0x0000000f
000010 0x0000001f
000020 0x00000027
Map...
Filter...
JTAG UART - jtag_uart
JTAG UART
Version 7.1
Documentation
1 Parameter Settings
Configuration
Simulation
Write FIFO (Data from Avalon to JTAG)
Buffer depth (bytes): 64
IRQ threshold: 8
Construct using registers instead of memory blocks
Read FIFO (Data from JTAG to Avalon)
Buffer depth (bytes): 64
IRQ threshold: 8
Construct using registers instead of memory blocks
Cancel
< Back
Next >
Finish
Warning: pio: PIO inputs are not hardwired in te
To Do: cpu: No reset vector has been specified
To Do: cpu: No exception vector has been spec
Exit
Help
Prev
Next
Generate
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera SOPC Buil...
10:18 PM


Altera SOPC Builder - nios_system.sopc (H:\SOPC_NiosIIfast\nios_system.sopc)
File Edit Module System View Tools Nios II Help
System Contents
System Generation
Altera SOPC Builder
Create new component...
Nios II Processor
Bridges and Adapters
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Ethernet
High Speed
PCI
Serial
JTAG UART
SPI (3 Wire Serial)
UART (RS-232 Serial Pc
Legacy Components
Memories and Memory Controllers
Peripherals
PLL
Add...
Target
Device Family: Cyclone II
Clock Settings
Name
Source
MHz
Pipeline
clk
External
50.0
Add
Remove
Use
Con...
Module Name
Description
Clock
Base
End
I...
cpu
Nios II Processor
instruction_master
Avalon Master
clk
data_master
Avalon Master
IRQ 0
IRQ 31
jtag_debug_module
Avalon Slave
0x00000800
0x00000fff
onchip_mem
On-Chip Memory (RAM or ROM)
s1
Avalon Slave
clk
0x00002000
0x00002fff
pio
PIO (Parallel I/O)
s1
Avalon Slave
clk
0x00000000
0x0000000f
pio_1
PIO (Parallel I/O)
s1
Avalon Slave
clk
0x00000010
0x0000001f
jtag_uart
JTAG UART
avalon_jtag_slave
Avalon Slave
clk
0x00000020
0x00000027
0
Remove
Edit...
Move Up
Move Down
Address Map...
Filter...
Warning: pio: PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.
To Do: cpu: No reset vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
To Do: cpu: No exception vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
Exit
Help
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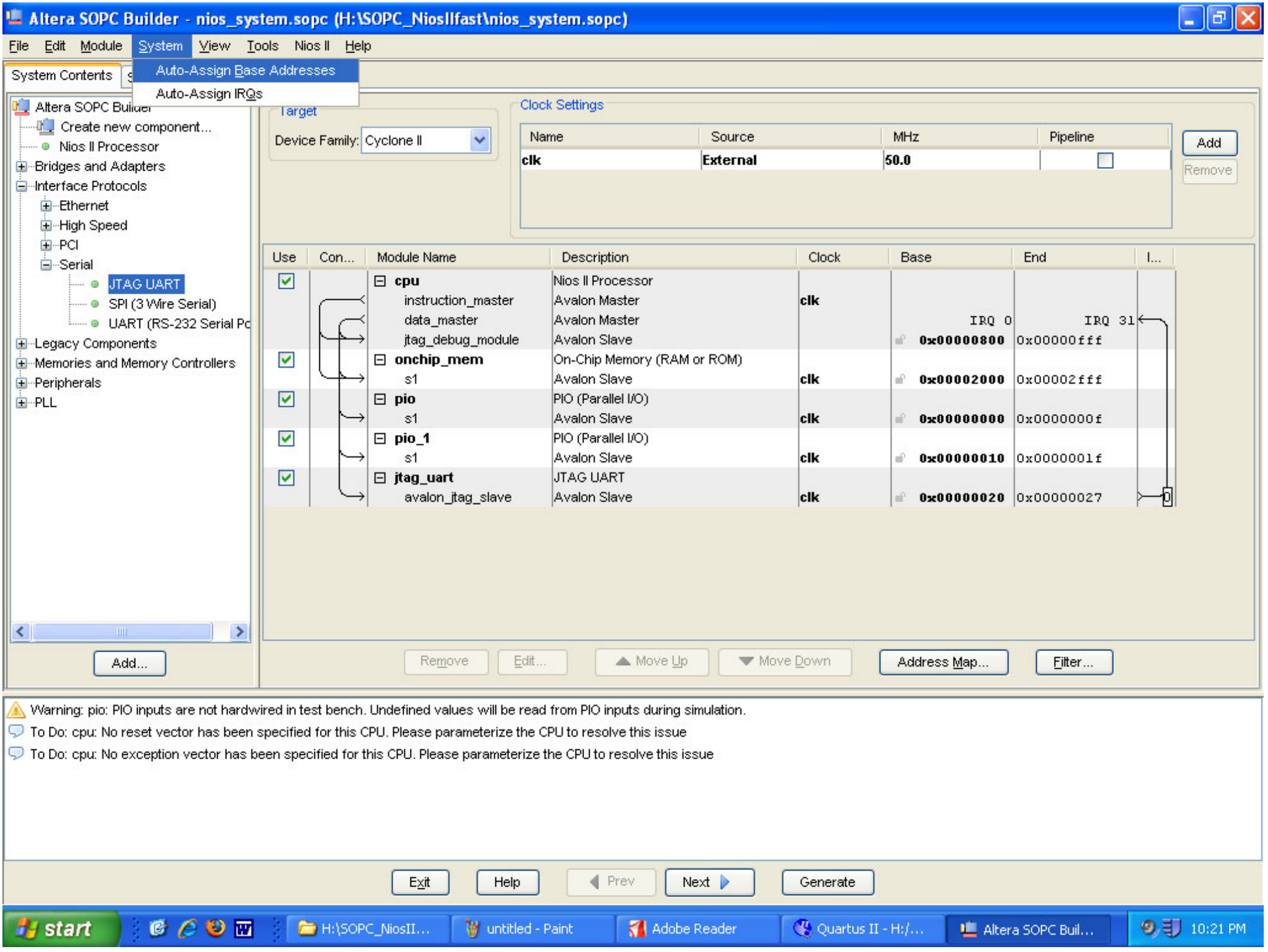
Next
Generate
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera SOPC Buil...
10:19 PM


Altera SOPC Builder - nios_system.sopc (H:\SOPC_NiosIIfast\nios_system.sopc)
File Edit Module System View Tools Nios II Help
Auto-Assign Base Addresses
Auto-Assign IRQs
System Contents
Create new component...
Nios II Processor
Bridges and Adapters
Interface Protocols
Ethernet
High Speed
PCI
Serial
JTAG UART
SPI (3 Wire Serial)
UART (RS-232 Serial Pc
Legacy Components
Memories and Memory Controllers
Peripherals
PLL
Add...
Target
Device Family: Cyclone II
Clock Settings
Name Source MHz Pipeline
clk External 50.0
Add
Remove
Use Con... Module Name Description Clock Base End I...
cpu Nios II Processor
instruction_master Avalon Master clk
data_master Avalon Master IRQ 0 IRQ 31
jtag_debug_module Avalon Slave 0x00000800 0x00000fff
onchip_mem On-Chip Memory (RAM or ROM)
s1 Avalon Slave clk 0x00002000 0x00002fff
pio PIO (Parallel I/O)
s1 Avalon Slave clk 0x00000000 0x0000000f
pio_1 PIO (Parallel I/O)
s1 Avalon Slave clk 0x00000010 0x0000001f
jtag_uart JTAG UART
avalon_jtag_slave Avalon Slave clk 0x00000020 0x00000027
Remove
Edit...
Move Up
Move Down
Address Map...
Filter...
Warning: pio: PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.
To Do: cpu: No reset vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
To Do: cpu: No exception vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
Exit
Help
Prev
Next
Generate
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera SOPC Buil...
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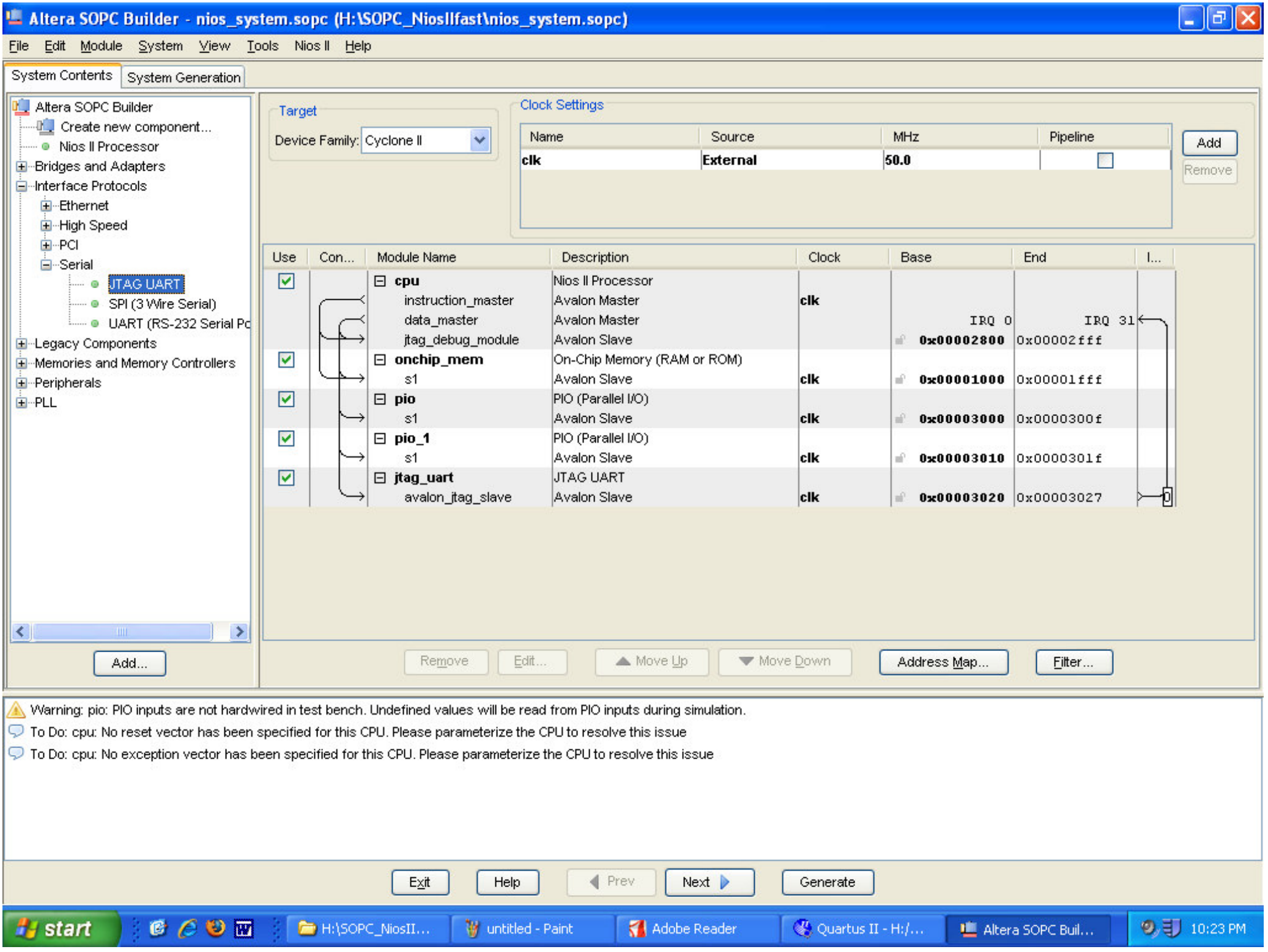
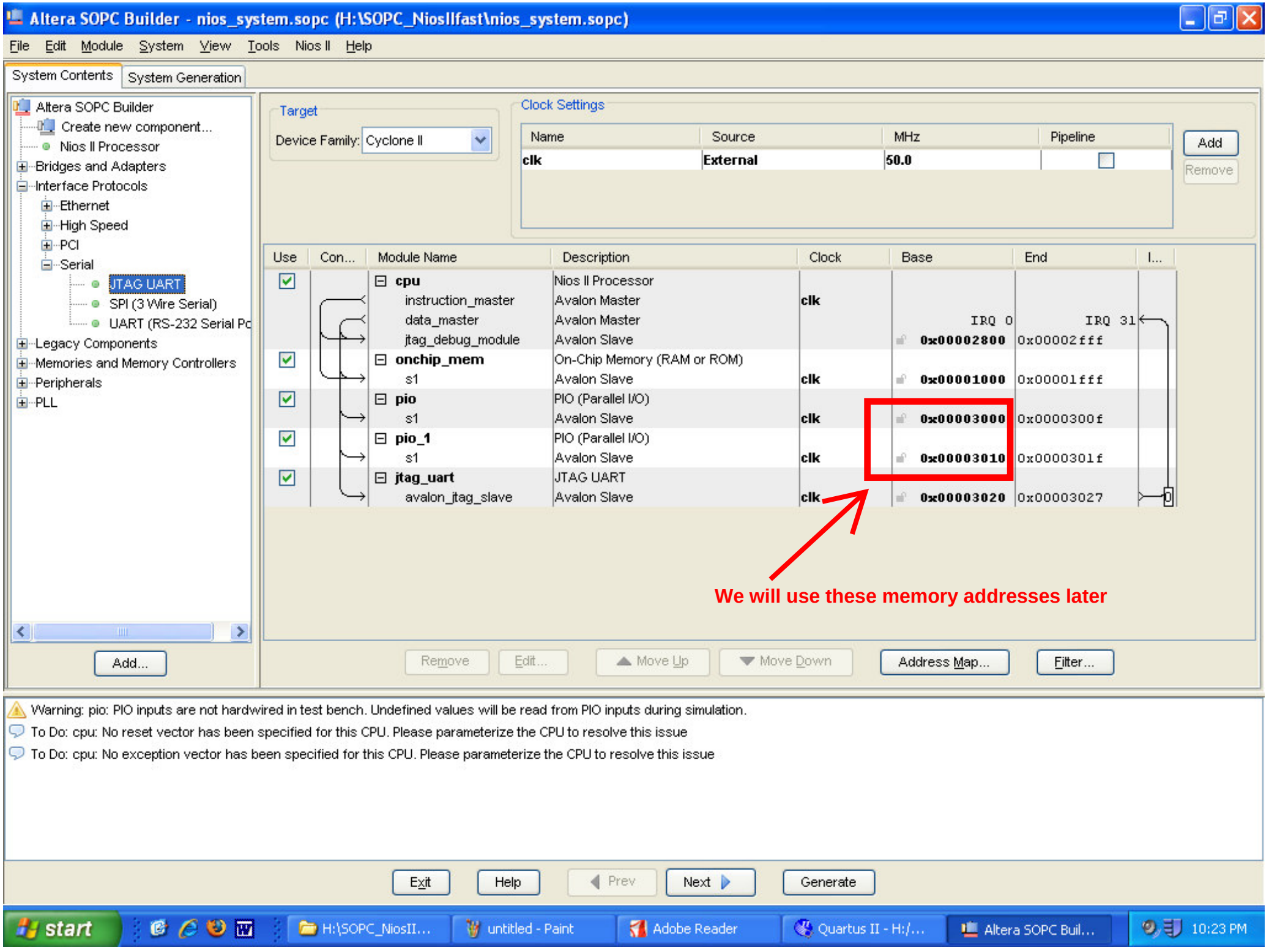

Altera SOPC Builder - nios_system.sopc (H:\SOPC_NiosIIfast\nios_system.sopc)
File Edit Module System View Tools Nios II Help
System Contents System Generation
Altera SOPC Builder
Create new component...
Nios II Processor
Bridges and Adapters
Interface Protocols
Ethernet
High Speed
PCI
Serial
JTAG UART
SPI (3 Wire Serial)
UART (RS-232 Serial Pc
Legacy Components
Memories and Memory Controllers
Peripherals
PLL
Add...
Target
Device Family: Cyclone II
Clock Settings
Name Source MHz Pipeline
clk External 50.0
Add
Remove
Use Con... Module Name Description Clock Base End I...
cpu Nios II Processor
instruction_master Avalon Master clk
data_master Avalon Master IRQ 0 IRQ 31
jtag_debug_module Avalon Slave 0x00002800 0x00002fff
onchip_mem On-Chip Memory (RAM or ROM)
s1 Avalon Slave clk 0x00001000 0x00001fff
pio PIO (Parallel I/O)
s1 Avalon Slave clk 0x00003000 0x0000300f
pio_1 PIO (Parallel I/O)
s1 Avalon Slave clk 0x00003010 0x0000301f
jtag_uart JTAG UART
avalon_jtag_slave Avalon Slave clk 0x00003020 0x00003027
0
Remove Edit... Move Up Move Down Address Map... Filter...
Warning: pio: PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.
To Do: cpu: No reset vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
To Do: cpu: No exception vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
Exit Help Prev Next Generate
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera SOPC Buil...
10:23 PM


Altera SOPC Builder - nios_system.sopc (H:\SOPC_NiosIIfast\nios_system.sopc)
File Edit Module System View Tools Nios II Help
System Contents System Generation
Altera SOPC Builder
Create new component...
Nios II Processor
Bridges and Adapters
Interface Protocols
Ethernet
High Speed
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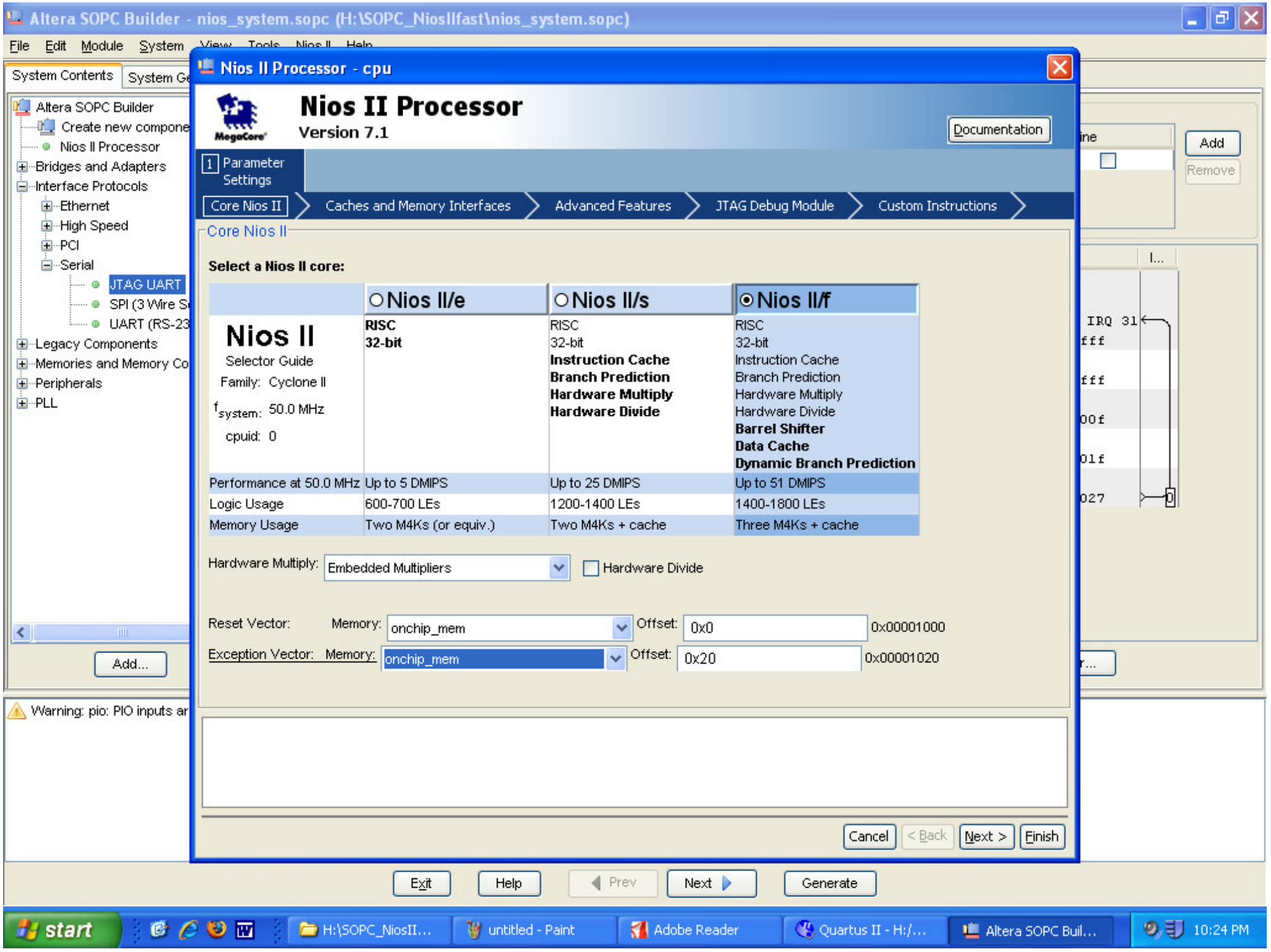
Serial
JTAG UART
SPI (3 Wire Serial)
UART (RS-232 Serial Pc
Legacy Components
Memories and Memory Controllers
Peripherals
PLL
Add...
Target
Device Family: Cyclone II
Clock Settings
Name Source MHz Pipeline
clk External 50.0
Add
Remove
Use Con... Module Name Description Clock Base End I...
cpu Nios II Processor
instruction_master Avalon Master clk
data_master Avalon Master IRQ 0 IRQ 31
jtag_debug_module Avalon Slave 0x00002800 0x00002fff
onchip_mem On-Chip Memory (RAM or ROM)
s1 Avalon Slave clk 0x00001000 0x00001fff
pio PIO (Parallel I/O)
s1 Avalon Slave clk 0x00003000 0x0000300f
pio_1 PIO (Parallel I/O)
s1 Avalon Slave clk 0x00003010 0x0000301f
jtag_uart JTAG UART
avalon_jtag_slave Avalon Slave clk 0x00003020 0x00003027
We will use these memory addresses later
Remove Edit... Move Up Move Down Address Map... Filter...
Warning: pio: PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.
To Do: cpu: No reset vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
To Do: cpu: No exception vector has been specified for this CPU. Please parameterize the CPU to resolve this issue
Exit Help Prev Next Generate
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera SOPC Buil...
10:23 PM


Altera SOPC Builder - nios_system.sopc (H:\SOPC_NiosIIfast\nios_system.sopc)
File Edit Module System View Tools Nios II Help
System Contents
Altera SOPC Builder
Create new compone
Nios II Processor
Bridges and Adapters
Interface Protocols
Ethernet
High Speed
PCI
Serial
JTAG UART
SPI (3 Wire S
UART (RS-23
Legacy Components
Memories and Memory Co
Peripherals
PLL
Add...
Warning: pio: PIO inputs ar
Nios II Processor - cpu
Nios II Processor
Version 7.1
Documentation
1 Parameter Settings
Core Nios II
Caches and Memory Interfaces
Advanced Features
JTAG Debug Module
Custom Instructions
Core Nios II
Select a Nios II core:
Nios II
Selector Guide
Family: Cyclone II
f system: 50.0 MHz
cpuid: 0
Nios II/e
RISC
32-bit
Nios II/s
RISC
32-bit
Instruction Cache
Branch Prediction
Hardware Multiply
Hardware Divide
Nios II/f
RISC
32-bit
Instruction Cache
Branch Prediction
Hardware Multiply
Hardware Divide
Barrel Shifter
Data Cache
Dynamic Branch Prediction
Performance at 50.0 MHz
Up to 5 DMIPS
Up to 25 DMIPS
Up to 51 DMIPS
Logic Usage
600-700 LEs
1200-1400 LEs
1400-1800 LEs
Memory Usage
Two M4Ks (or equiv.)
Two M4Ks + cache
Three M4Ks + cache
Hardware Multiply: Embedded Multipliers
Hardware Divide
Reset Vector: Memory: onchip_mem Offset: 0x0 0x00001000
Exception Vector: Memory: onchip_mem Offset: 0x20 0x00001020
Cancel
< Back
Next >
Finish
Add
Remove
IRQ 31
Exit
Help
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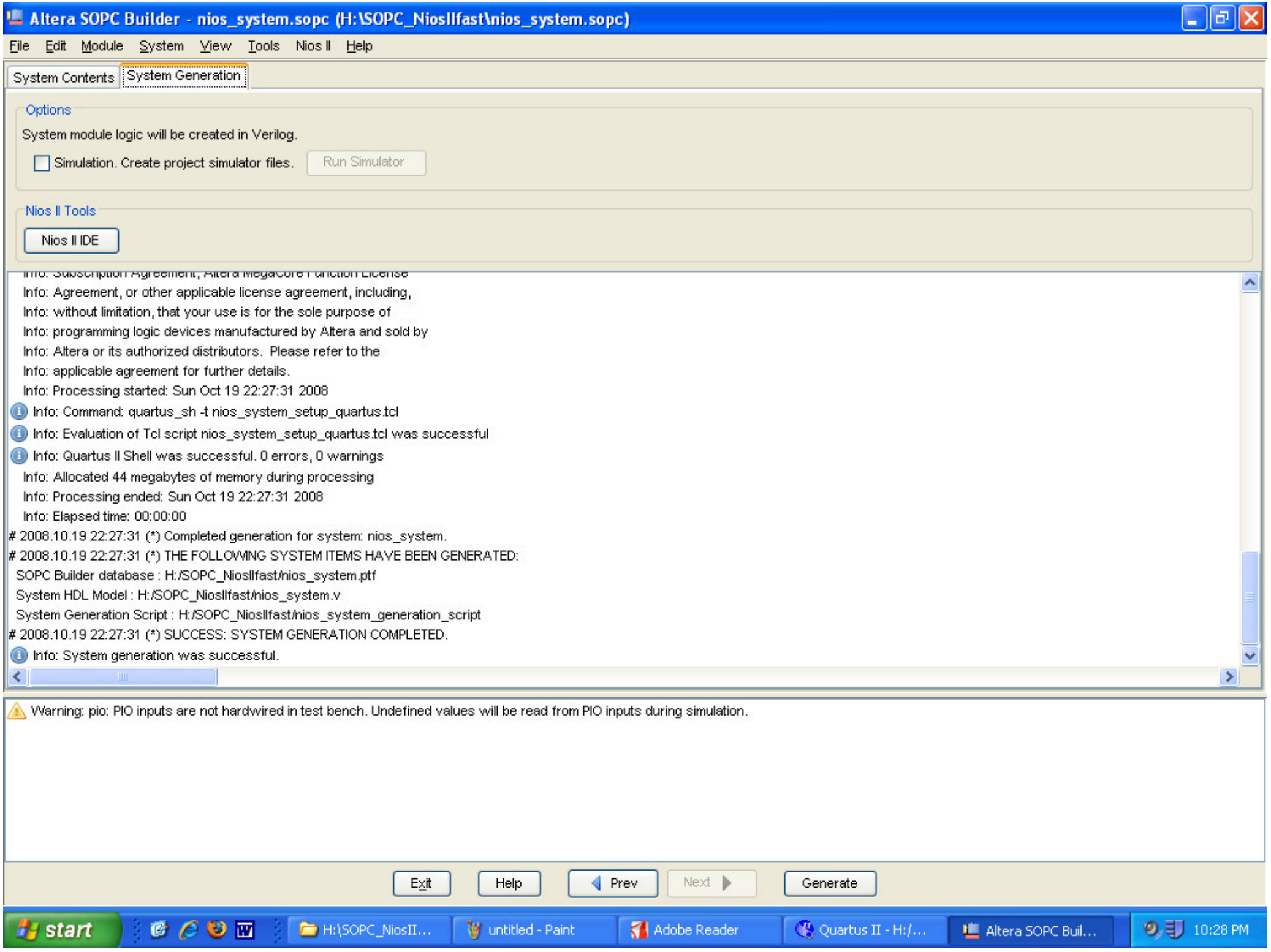
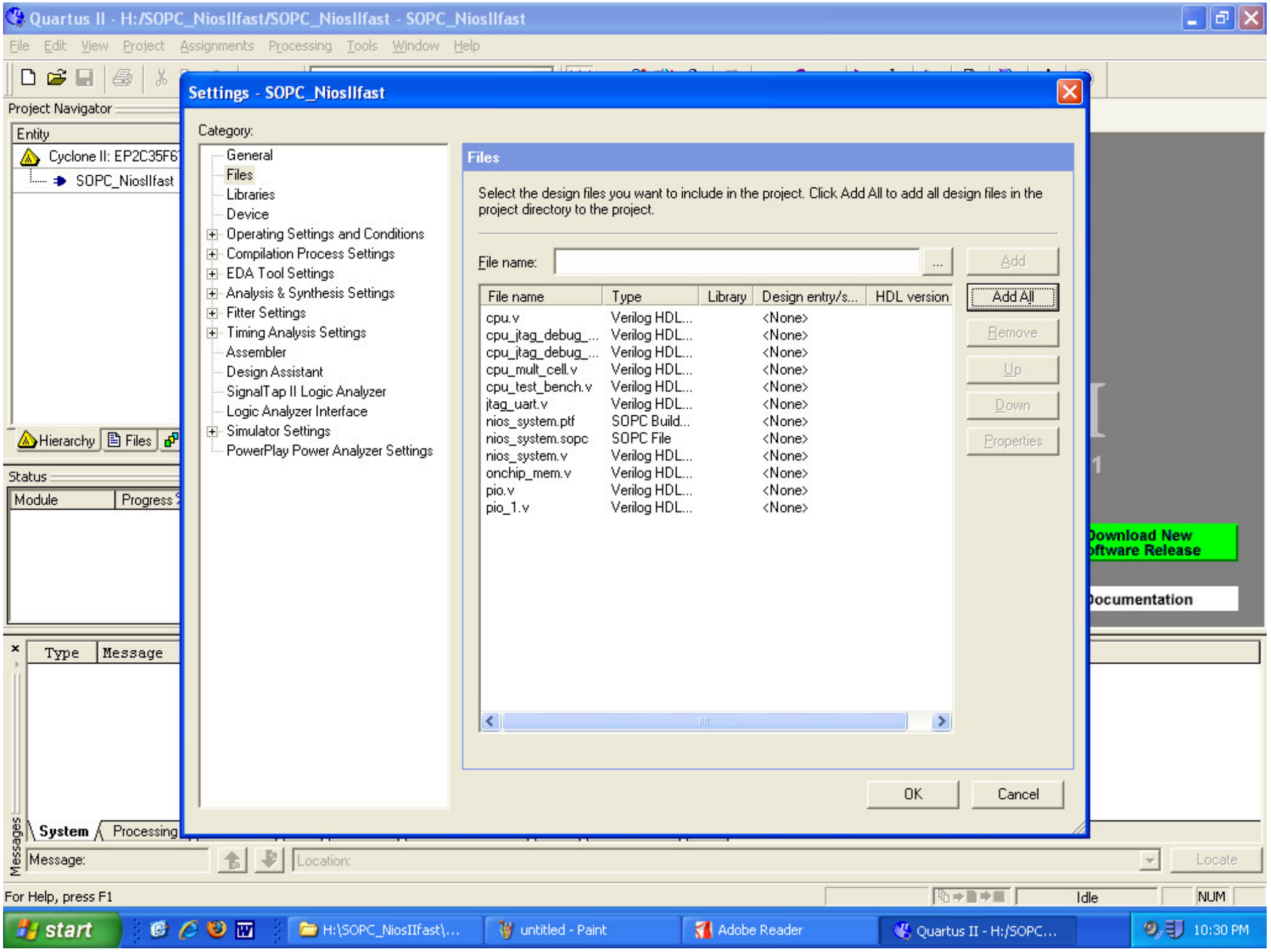
Next
Generate
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera SOPC Buil...
10:24 PM


Altera SOPC Builder - nios_system.sopc (H:\SOPC_NiosIIfast\nios_system.sopc)
File Edit Module System View Tools Nios II Help
System Contents System Generation
Options
System module logic will be created in Verilog.
Simulation. Create project simulator files.
Run Simulator
Nios II Tools
Nios II IDE
Info: Agreement, or other applicable license agreement, including,
Info: without limitation, that your use is for the sole purpose of
Info: programming logic devices manufactured by Altera and sold by
Info: Altera or its authorized distributors. Please refer to the
Info: applicable agreement for further details.
Info: Processing started: Sun Oct 19 22:27:31 2008
Info: Command: quartus_sh -t nios_system_setup_quartus.tcl
Info: Evaluation of Tcl script nios_system_setup_quartus.tcl was successful
Info: Quartus II Shell was successful. 0 errors, 0 warnings
Info: Allocated 44 megabytes of memory during processing
Info: Processing ended: Sun Oct 19 22:27:31 2008
Info: Elapsed time: 00:00:00
2008.10.19 22:27:31 (*) Completed generation for system: nios_system.
2008.10.19 22:27:31 (*) THE FOLLOWING SYSTEM ITEMS HAVE BEEN GENERATED:
SOPC Builder database : H:/SOPC_NiosIIfast/nios_system.ptf
System HDL Model : H:/SOPC_NiosIIfast/nios_system.v
System Generation Script : H:/SOPC_NiosIIfast/nios_system_generation_script
2008.10.19 22:27:31 (*) SUCCESS: SYSTEM GENERATION COMPLETED.
Info: System generation was successful.
Warning: pio: PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.
Exit
Help
Prev
Next
Generate
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera SOPC Buil...
10:28 PM

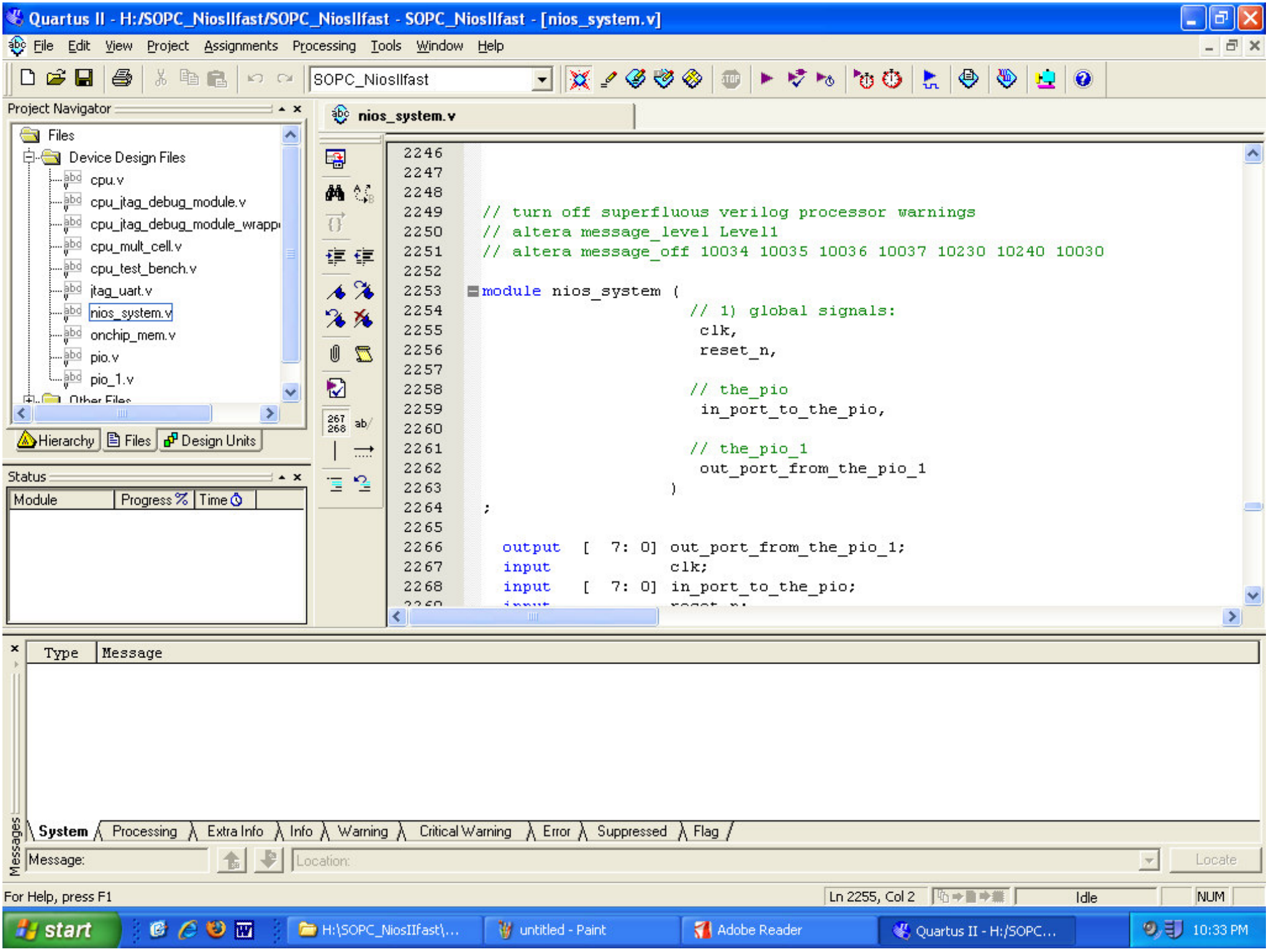

Quartus II - H:/SOPC_NiosIIfast/SOPC_NiosIIfast - SOPC_NiosIIfast
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Cyclone II: EP2C35F6
SOPC_NiosIIfast
Hierarchy Files
Status
Module Progress
Type Message
System Processing
Message:
Location:
Locate
For Help, press F1
Idle
NUM
Settings - SOPC_NiosIIfast
Category:
General
Files
Libraries
Device
Operating Settings and Conditions
Compilation Process Settings
EDA Tool Settings
Analysis & Synthesis Settings
Fitter Settings
Timing Analysis Settings
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
Simulator Settings
PowerPlay Power Analyzer Settings
Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
File name:
Add
Add All
Remove
Up
Down
Properties
File name Type Library Design entry/s... HDL version
cpu.v Verilog HDL... <None>
cpu_jtag_debug_... Verilog HDL... <None>
cpu_jtag_debug_... Verilog HDL... <None>
cpu_mult_cell.v Verilog HDL... <None>
cpu_test_bench.v Verilog HDL... <None>
jtag_uart.v Verilog HDL... <None>
nios_system.ptf SOPC Build... <None>
nios_system.sopc SOPC File <None>
nios_system.v Verilog HDL... <None>
onchip_mem.v Verilog HDL... <None>
pio.v Verilog HDL... <None>
pio_1.v Verilog HDL... <None>
OK
Cancel
Download New
oftware Release
Documentation
start
H:\SOPC_NiosIIfast\...
untitled - Paint
Adobe Reader
Quartus II - H:/SOPC...
10:30 PM

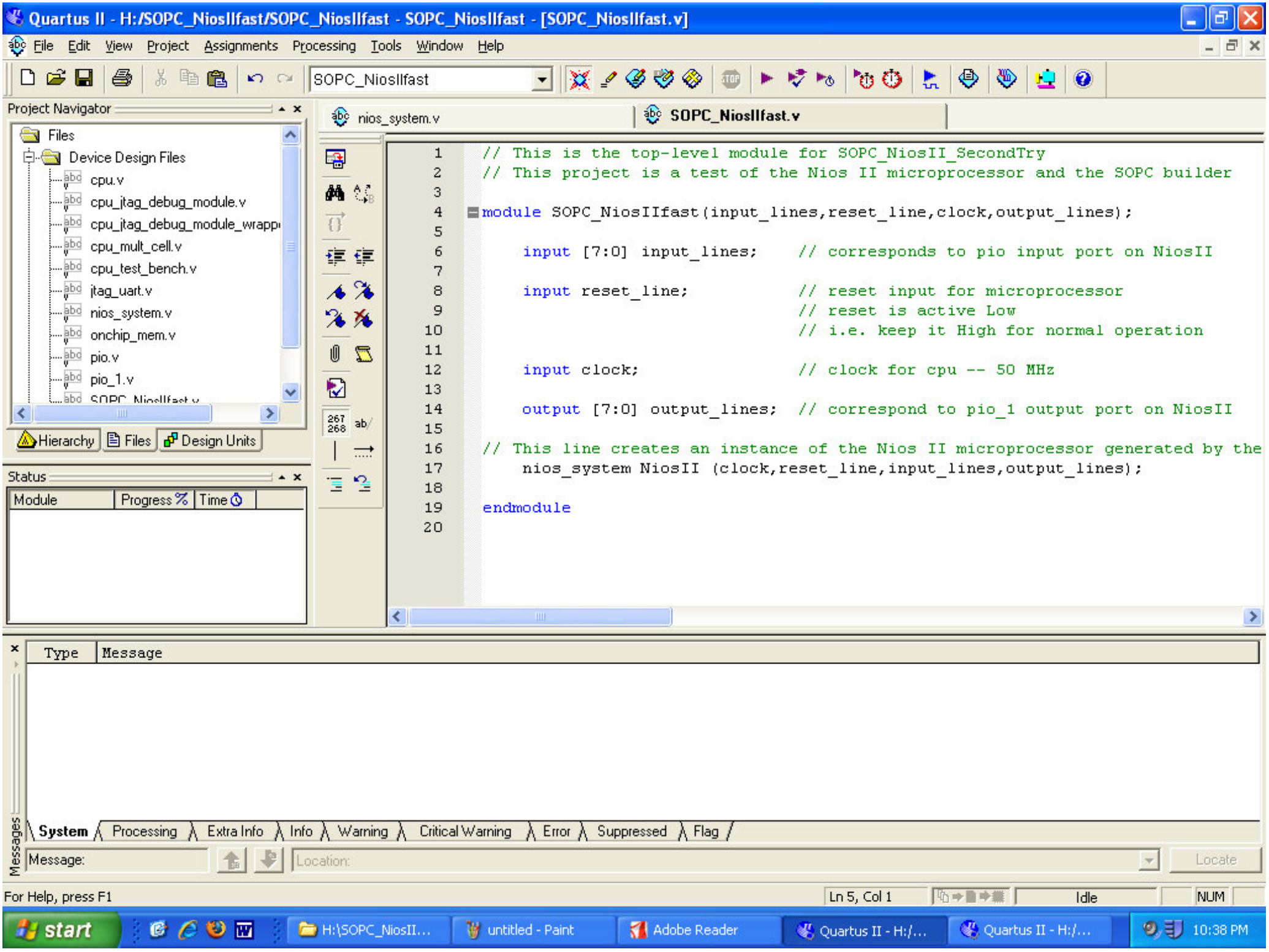
Main Nios II module is called

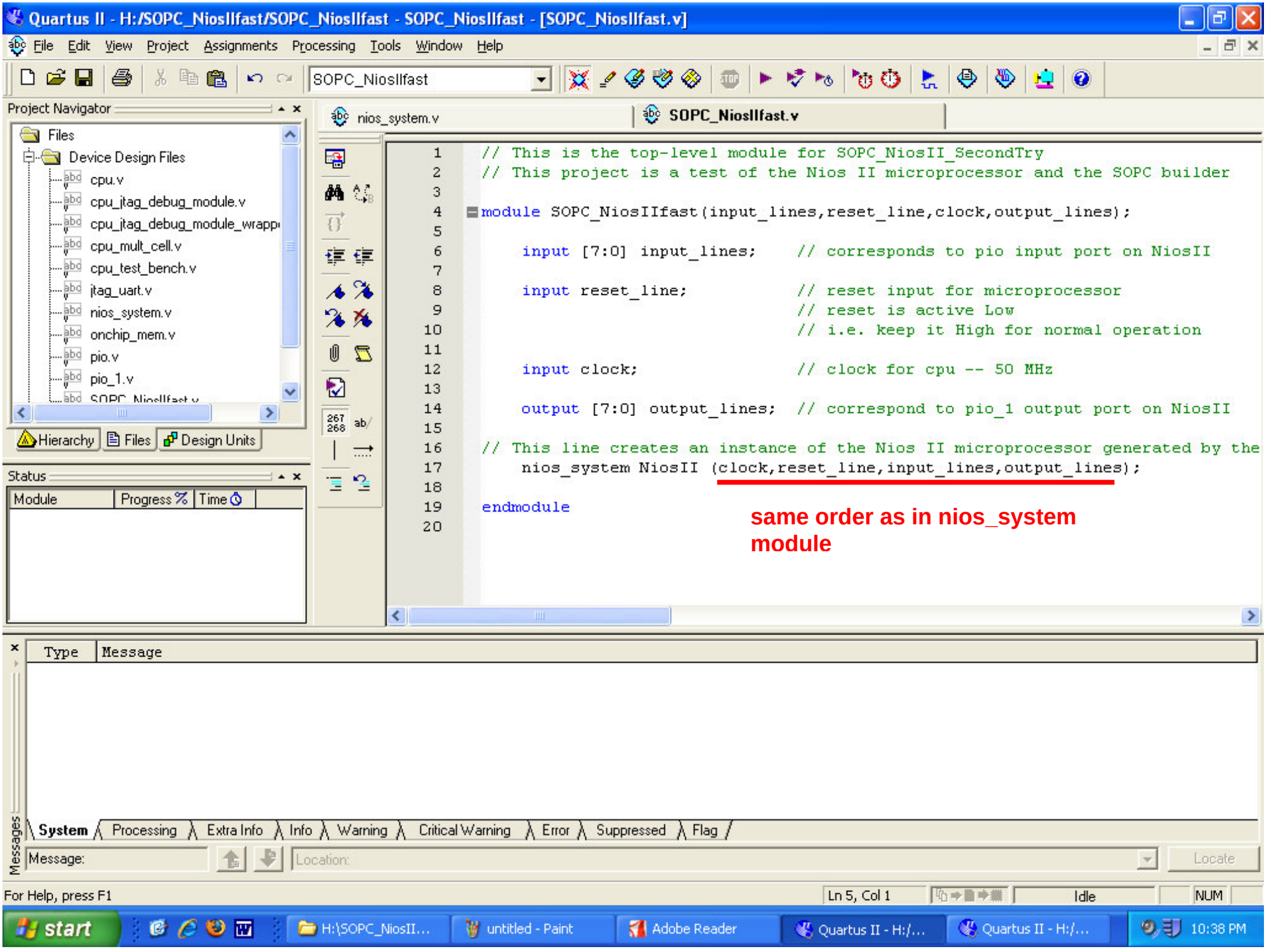
nios_system

The code for nios_system is in

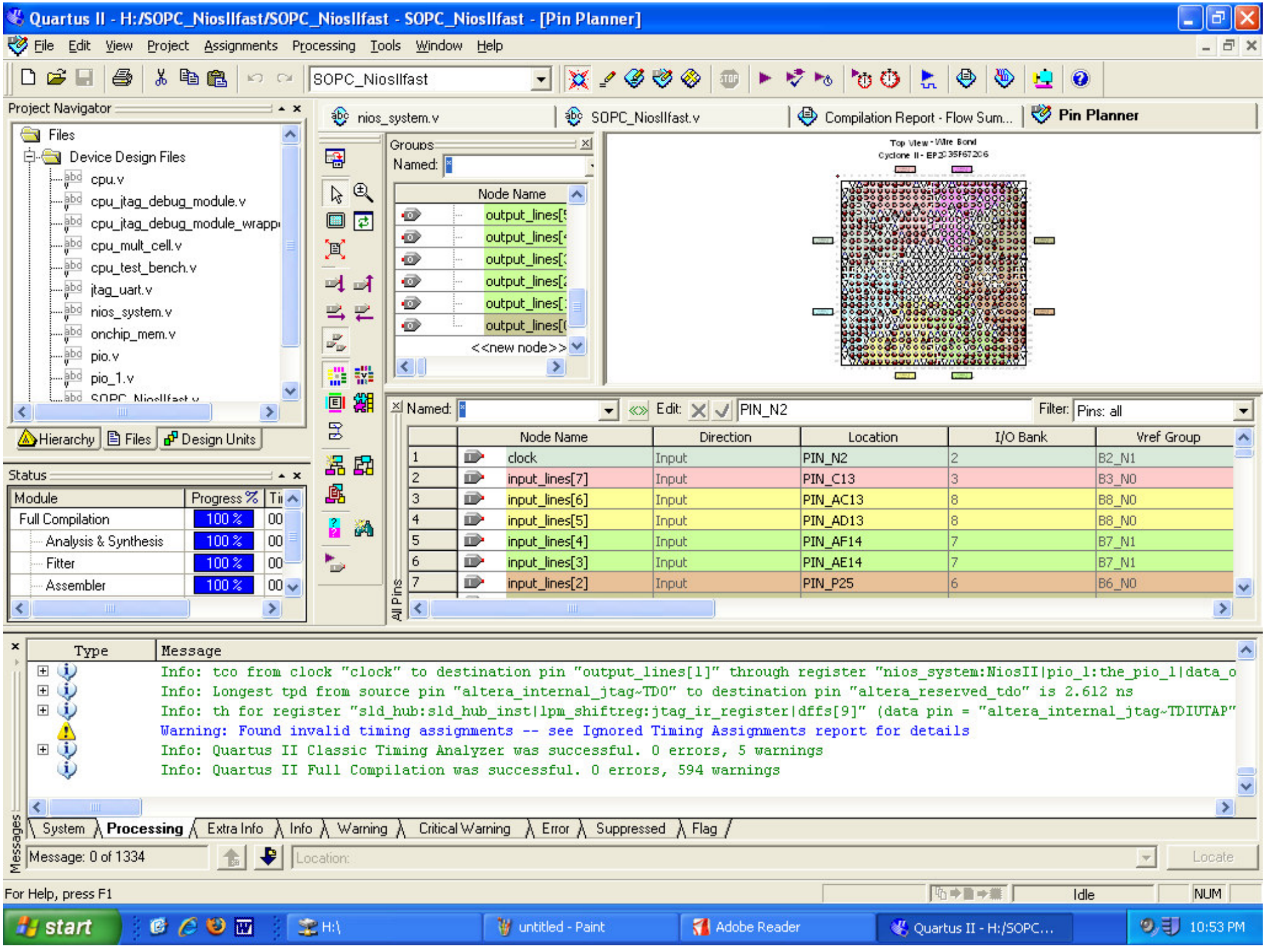
nios_system.v

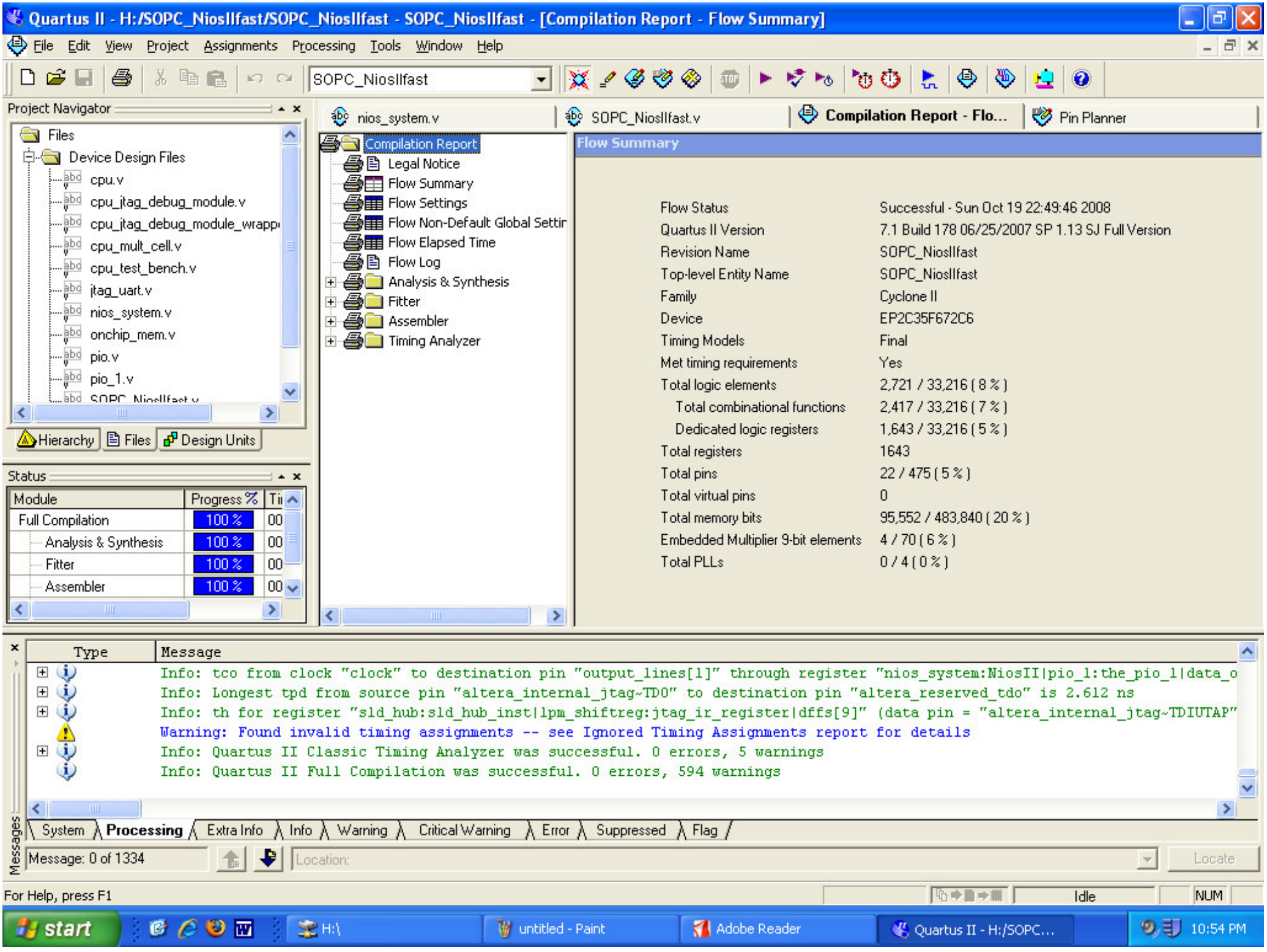

Quartus II - H:/SOPC_NiosIIfast/SOPC_NiosIIfast - SOPC_NiosIIfast - [nios_system.v]
File Edit View Project Assignments Processing Tools Window Help
SOPC_NiosIIfast
Project Navigator
Files
Device Design Files
cpu.v
cpu_jtag_debug_module.v
cpu_jtag_debug_module_wrapp
cpu_mult_cell.v
cpu_test_bench.v
jtag_uart.v
nios_system.v
onchip_mem.v
pio.v
pio_1.v
Hierarchy Files Design Units
Status
Module Progress Time
nios_system.v
2246
2247
2248
2249 // turn off superfluous verilog processor warnings
2250 // altera message_level Level1
2251 // altera message_off 10034 10035 10036 10037 10230 10240 10030
2252
2253 module nios_system (
2254 // 1) global signals:
2255 clk,
2256 reset_n,
2257
2258 // the_pio
2259 in_port_to_the_pio,
2260
2261 // the_pio_1
2262 out_port_from_the_pio_1
2263)
2264 ;
2265
2266 output [7: 0] out_port_from_the_pio_1;
2267 input clk;
2268 input [7: 0] in_port_to_the_pio;
Type Message
System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag
Message: Location: Locate
Messages
For Help, press F1
Ln 2255, Col 2
Idle
NUM
start
H:\SOPC_NiosIIfast\...
untitled - Paint
Adobe Reader
Quartus II - H:/SOPC...
10:33 PM

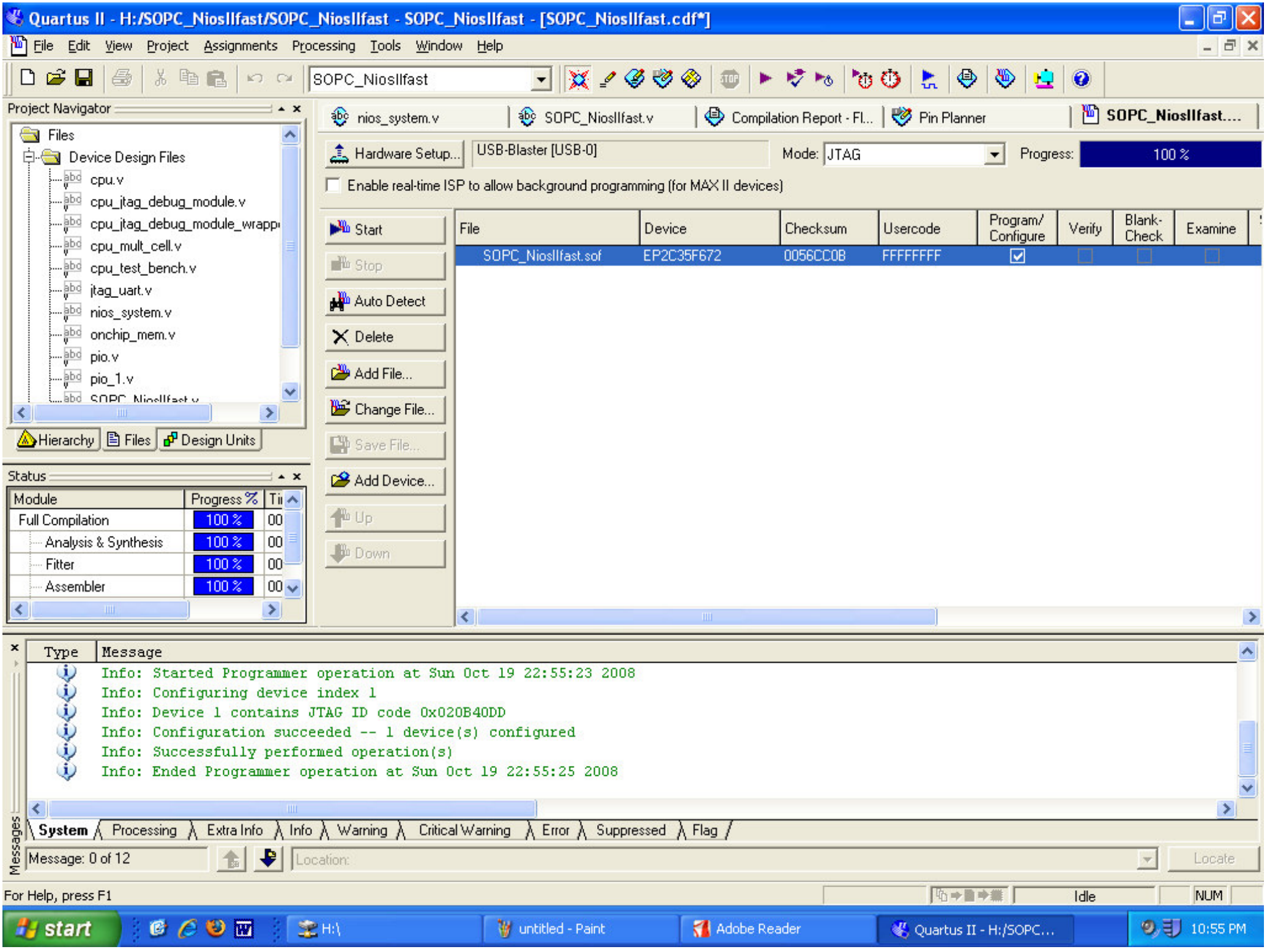

Quartus II - H:/SOPC_NiosIIfast/SOPC_NiosIIfast - SOPC_NiosIIfast - [SOPC_NiosIIfast.v]
File Edit View Project Assignments Processing Tools Window Help
SOPC_NiosIIfast
Project Navigator
Files
Device Design Files
cpu.v
cpu_jtag_debug_module.v
cpu_jtag_debug_module_wrapp
cpu_mult_cell.v
cpu_test_bench.v
jtag_uart.v
nios_system.v
onchip_mem.v
pio.v
pio_1.v
SOPC_NiosIIfast.v
Hierarchy
Files
Design Units
Status
Module
Progress
Time
nios_system.v
SOPC_NiosIIfast.v
1 // This is the top-level module for SOPC_NiosII_SecondTry
2 // This project is a test of the Nios II microprocessor and the SOPC builder
3
4 module SOPC_NiosIIfast(input_lines,reset_line,clock,output_lines);
5
6 input [7:0] input_lines; // corresponds to pio input port on NiosII
7
8 input reset_line; // reset input for microprocessor
9 // reset is active Low
10 // i.e. keep it High for normal operation
11
12 input clock; // clock for cpu -- 50 MHz
13
14 output [7:0] output_lines; // correspond to pio_1 output port on NiosII
15
16 // This line creates an instance of the Nios II microprocessor generated by the
17 nios_system NiosII (clock,reset_line,input_lines,output_lines);
18
19 endmodule
20
Type
Message
System
Processing
Extra Info
Info
Warning
Critical Warning
Error
Suppressed
Flag
Messages
Message:
Location:
Locate
For Help, press F1
Ln 5, Col 1
Idle
NUM
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Quartus II - H:/...
10:38 PM


Quartus II - H:/SOPC_NiosIIfast/SOPC_NiosIIfast - SOPC_NiosIIfast - [SOPC_NiosIIfast.v]
File Edit View Project Assignments Processing Tools Window Help
SOPC_NiosIIfast
Project Navigator
Files
Device Design Files
cpu.v
cpu_jtag_debug_module.v
cpu_jtag_debug_module_wrapp
cpu_mult_cell.v
cpu_test_bench.v
jtag_uart.v
nios_system.v
onchip_mem.v
pio.v
pio_1.v
Hierarchy
Files
Design Units
Status
Module
Progress
Time
nios_system.v
SOPC_NiosIIfast.v
1 // This is the top-level module for SOPC_NiosII_SecondTry
2 // This project is a test of the Nios II microprocessor and the SOPC builder
3
4 module SOPC_NiosIIfast(input_lines,reset_line,clock,output_lines);
5
6 input [7:0] input_lines; // corresponds to pio input port on NiosII
7
8 input reset_line; // reset input for microprocessor
9 // reset is active Low
10 // i.e. keep it High for normal operation
11
12 input clock; // clock for cpu -- 50 MHz
13
14 output [7:0] output_lines; // correspond to pio_1 output port on NiosII
15
16 // This line creates an instance of the Nios II microprocessor generated by the
17 nios_system NiosII (clock,reset_line,input_lines,output_lines);
18
19 endmodule
20
same order as in nios_system module
Type
Message
System
Processing
Extra Info
Info
Warning
Critical Warning
Error
Suppressed
Flag
Messages
Message:
Location:
Locate
For Help, press F1
Ln 5, Col 1
Idle
NUM
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Quartus II - H:/...
10:38 PM

Compile project (1st compilation)


Quartus II - H:/SOPC_NiosIIfast/SOPC_NiosIIfast - SOPC_NiosIIfast - [Pin Planner]
File Edit View Project Assignments Processing Tools Window Help
SOPC_NiosIIfast
Project Navigator
Files
Device Design Files
cpu.v
cpu_jtag_debug_module.v
cpu_mult_cell.v
cpu_test_bench.v
jtag_uart.v
nios_system.v
onchip_mem.v
pio.v
pio_1.v
Hierarchy Files Design Units
nios_system.v
SOPC_NiosIIfast.v
Compilation Report - Flow Sum...
Pin Planner
Groups
Named:
Node Name
output_lines[5]
output_lines[4]
output_lines[3]
output_lines[2]
output_lines[1]
output_lines[0]
<<new node>>
Top View - Wire Bond
Cyclone II - EP2C35F672C6
Status
Module Progress %
Full Compilation 100 %
Analysis & Synthesis 100 %
Fitter 100 %
Assembler 100 %
Named: Edit: PIN_N2 Filter: Pins: all
All Pins
1 clock Input PIN_N2 2 B2_N1
2 input_lines[7] Input PIN_C13 3 B3_N0
3 input_lines[6] Input PIN_AC13 8 B8_N0
4 input_lines[5] Input PIN_AD13 8 B8_N0
5 input_lines[4] Input PIN_AF14 7 B7_N1
6 input_lines[3] Input PIN_AE14 7 B7_N1
7 input_lines[2] Input PIN_P25 6 B6_N0
Type Message
Info: tco from clock "clock" to destination pin "output_lines[1]" through register "nios_system:NiosII|pio_1:the_pio_1|data_o
Info: Longest tpd from source pin "altera_internal_jtag~TDO" to destination pin "altera_reserved_tdo" is 2.612 ns
Info: th for register "sld_hub:sld_hub_inst|lpm_shiftreg:jtag_ir_register|dffs[9]" (data pin = "altera_internal_jtag~TDIUTAP"
Warning: Found invalid timing assignments -- see Ignored Timing Assignments report for details
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 5 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 594 warnings
Messages
System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag
Message: 0 of 1334
Location:
Locate
For Help, press F1
Idle
NUM
start
H:\
untitled - Paint
Adobe Reader
Quartus II - H:/SOPC...
10:53 PM


Quartus II - H:/SOPC_NiosIIfast/SOPC_NiosIIfast - SOPC_NiosIIfast - [Compilation Report - Flow Summary]
File Edit View Project Assignments Processing Tools Window Help
SOPC_NiosIIfast
Project Navigator
Files
Device Design Files
cpu.v
cpu_jtag_debug_module.v
cpu_jtag_debug_module_wrapp
cpu_mult_cell.v
cpu_test_bench.v
jtag_uart.v
nios_system.v
onchip_mem.v
pio.v
pio_1.v
Hierarchy Files Design Units
Status
Module Progress %
Full Compilation 100 %
Analysis & Synthesis 100 %
Fitter 100 %
Assembler 100 %
nios_system.v
SOPC_NiosIIfast.v
Compilation Report - Flo...
Pin Planner
Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global Settir
Flow Elapsed Time
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
Flow Summary
Flow Status Successful - Sun Oct 19 22:49:46 2008
Quartus II Version 7.1 Build 178 06/25/2007 SP 1.13 SJ Full Version
Revision Name SOPC_NiosIIfast
Top-level Entity Name SOPC_NiosIIfast
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Met timing requirements Yes
Total logic elements 2,721 / 33,216 (8 %)
Total combinational functions 2,417 / 33,216 (7 %)
Dedicated logic registers 1,643 / 33,216 (5 %)
Total registers 1643
Total pins 22 / 475 (5 %)
Total virtual pins 0
Total memory bits 95,552 / 483,840 (20 %)
Embedded Multiplier 9-bit elements 4 / 70 (6 %)
Total PLLs 0 / 4 (0 %)
Type Message
Info: tco from clock "clock" to destination pin "output_lines[1]" through register "nios_system:NiosII|pio_1:the_pio_1|data_o
Info: Longest tpd from source pin "altera_internal_jtag~TDO" to destination pin "altera_reserved_tdo" is 2.612 ns
Info: th for register "sld_hub:sld_hub_inst|lpm_shiftreg:jtag_ir_register|dffs[9]" (data pin = "altera_internal_jtag~TDIUTAP"
Warning: Found invalid timing assignments -- see Ignored Timing Assignments report for details
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 5 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 594 warnings
Messages
System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag
Message: 0 of 1334
Location:
Locate
For Help, press F1
Idle
NUM
start
H:\
untitled - Paint
Adobe Reader
Quartus II - H:/SOPC...
10:54 PM

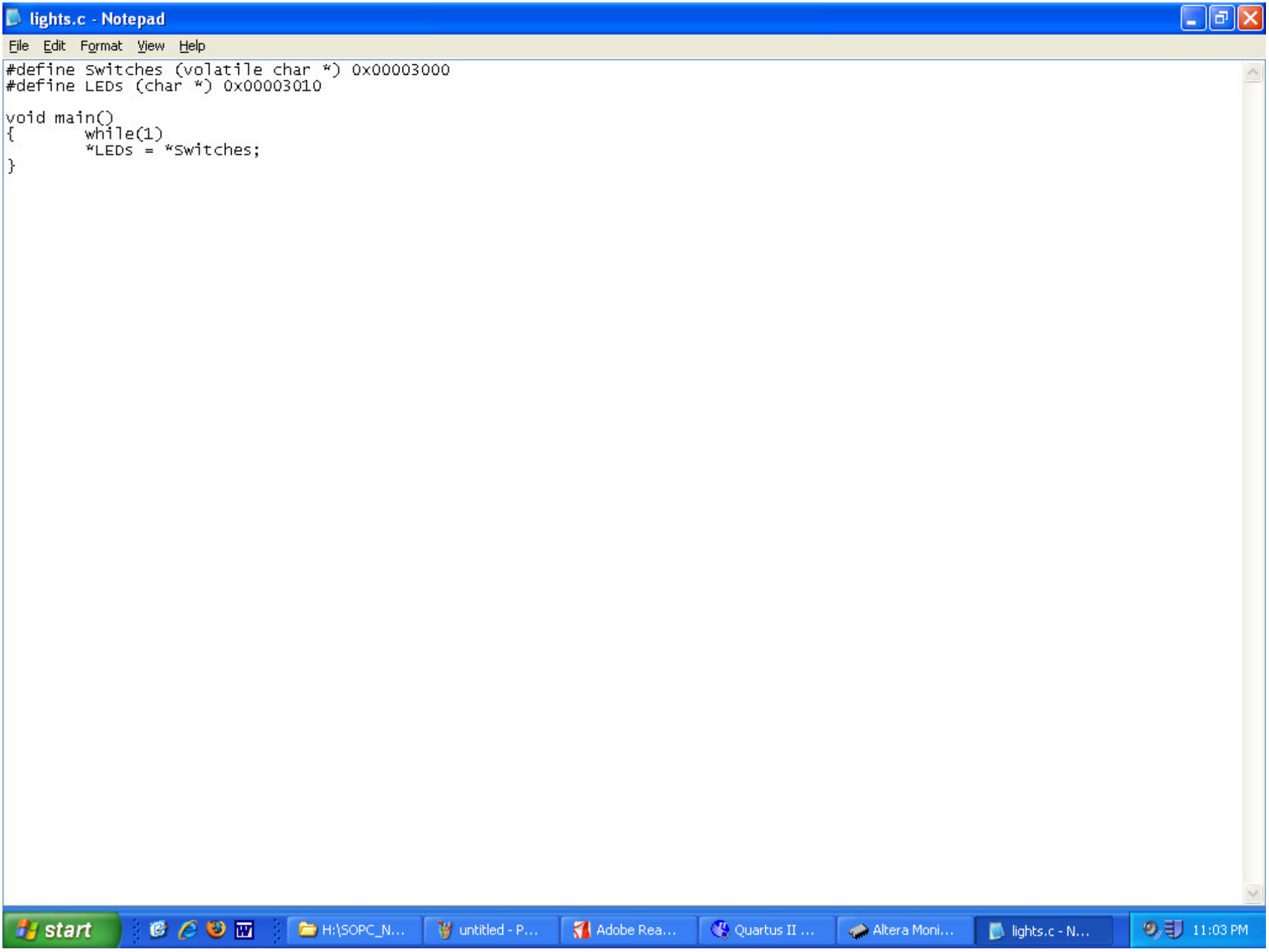

Quartus II - H:/SOPC_NiosIIfast/SOPC_NiosIIfast - SOPC_NiosIIfast - [SOPC_NiosIIfast.cdf*]
File Edit View Project Assignments Processing Tools Window Help
SOPC_NiosIIfast
Project Navigator
Files
Device Design Files
cpu.v
cpu_jtag_debug_module.v
cpu_jtag_debug_module_wrapp
cpu_mult_cell.v
cpu_test_bench.v
jtag_uart.v
nios_system.v
onchip_mem.v
pio.v
pio_1.v
Hierarchy
Files
Design Units
Status
Module
Progress %
Full Compilation
Analysis & Synthesis
Fitter
Assembler
100 %
nios_system.v
SOPC_NiosIIfast.v
Compilation Report - Fl...
Pin Planner
SOPC_NiosIIfast....
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
100 %
Enable real-time ISP to allow background programming (for MAX II devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File...
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
SOPC_NiosIIfast.sof
EP2C35F672
0056CC0B
FFFFFFFF
Type
Message
Info: Started Programmer operation at Sun Oct 19 22:55:23 2008
Info: Configuring device index 1
Info: Device 1 contains JTAG ID code 0x020B40DD
Info: Configuration succeeded -- 1 device(s) configured
Info: Successfully performed operation(s)
Info: Ended Programmer operation at Sun Oct 19 22:55:25 2008
System
Processing
Extra Info
Info
Warning
Critical Warning
Error
Suppressed
Flag
Messages
Message: 0 of 12
Location:
Locate
For Help, press F1
Idle
NUM
start
H:\
untitled - Paint
Adobe Reader
Quartus II - H:/SOPC...
10:55 PM

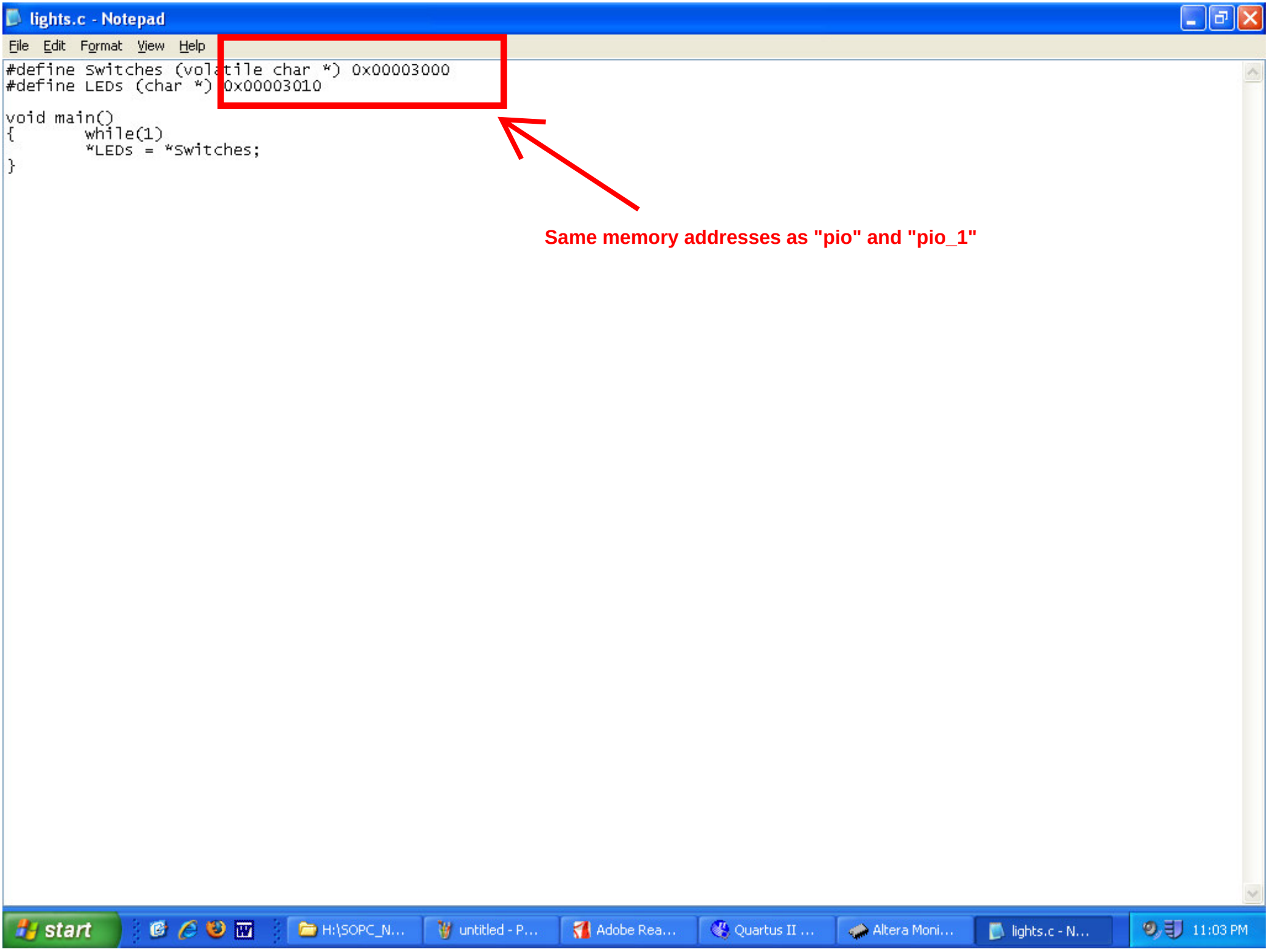
Programming Nios II

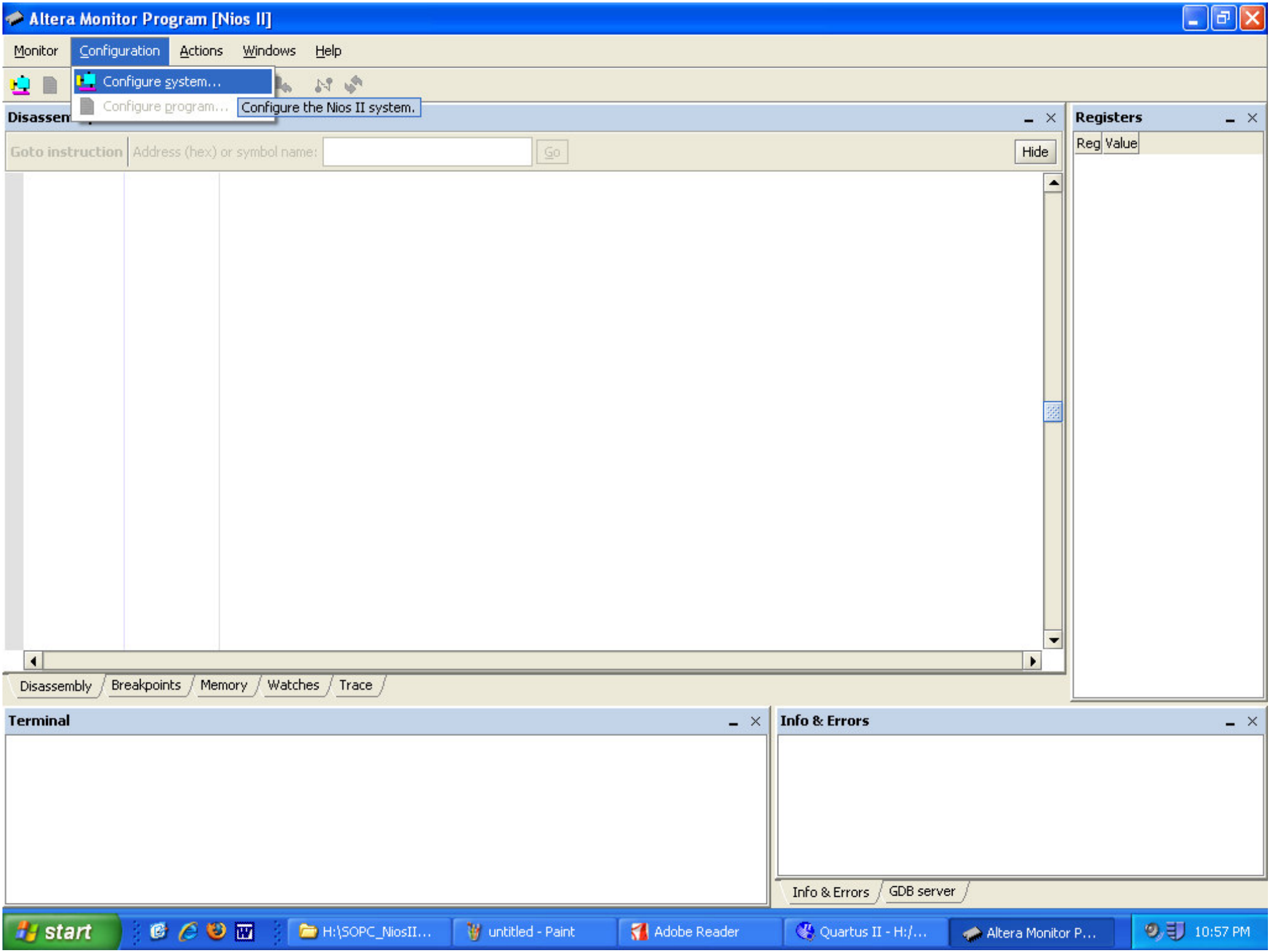
We will use the **Altera Monitor Program** is used to download a program into the Nios II microprocessor embedded in the FPGA. It uses the JTAG protocol.

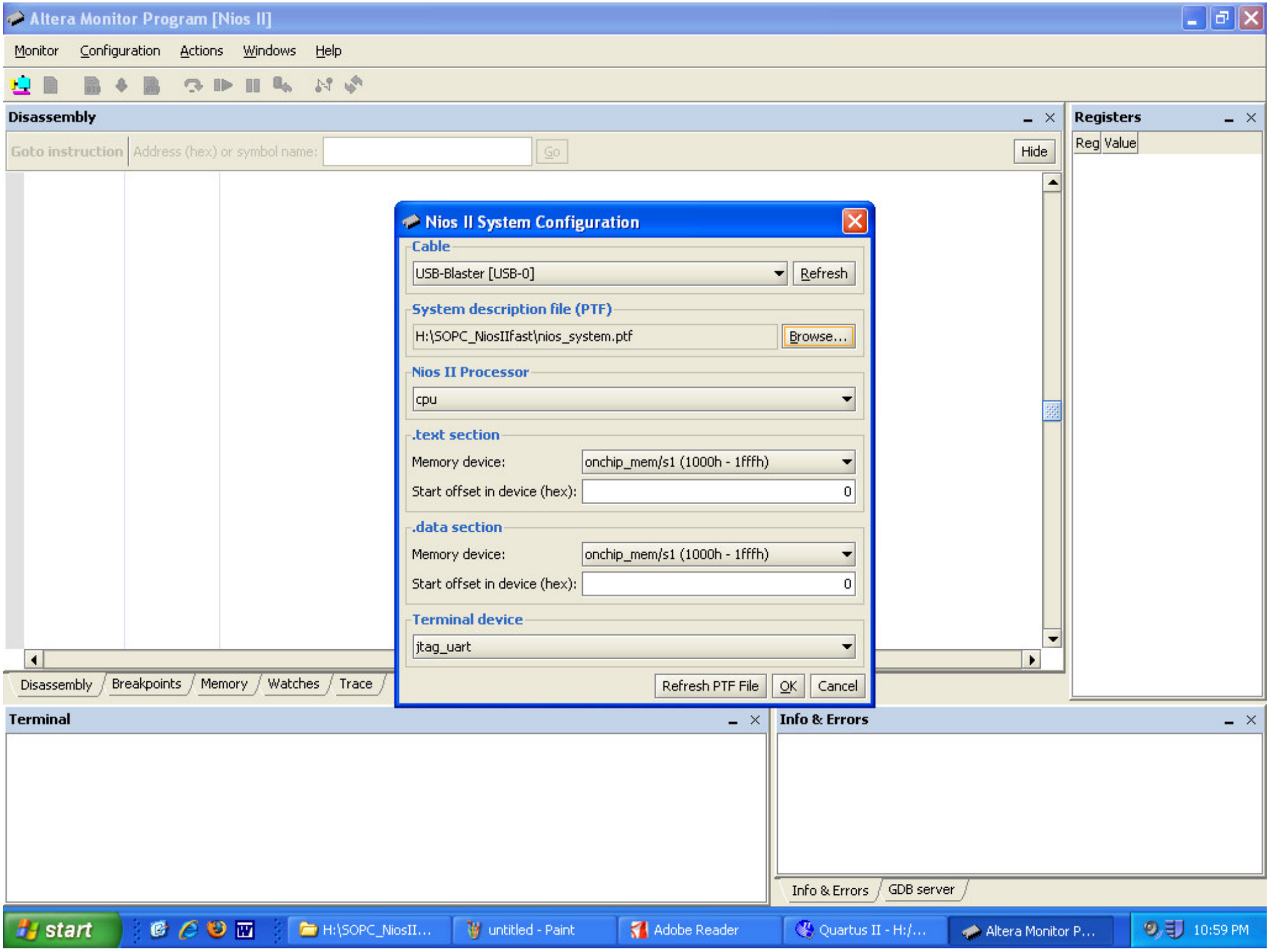
→ We will program with C (the post popular programming language).

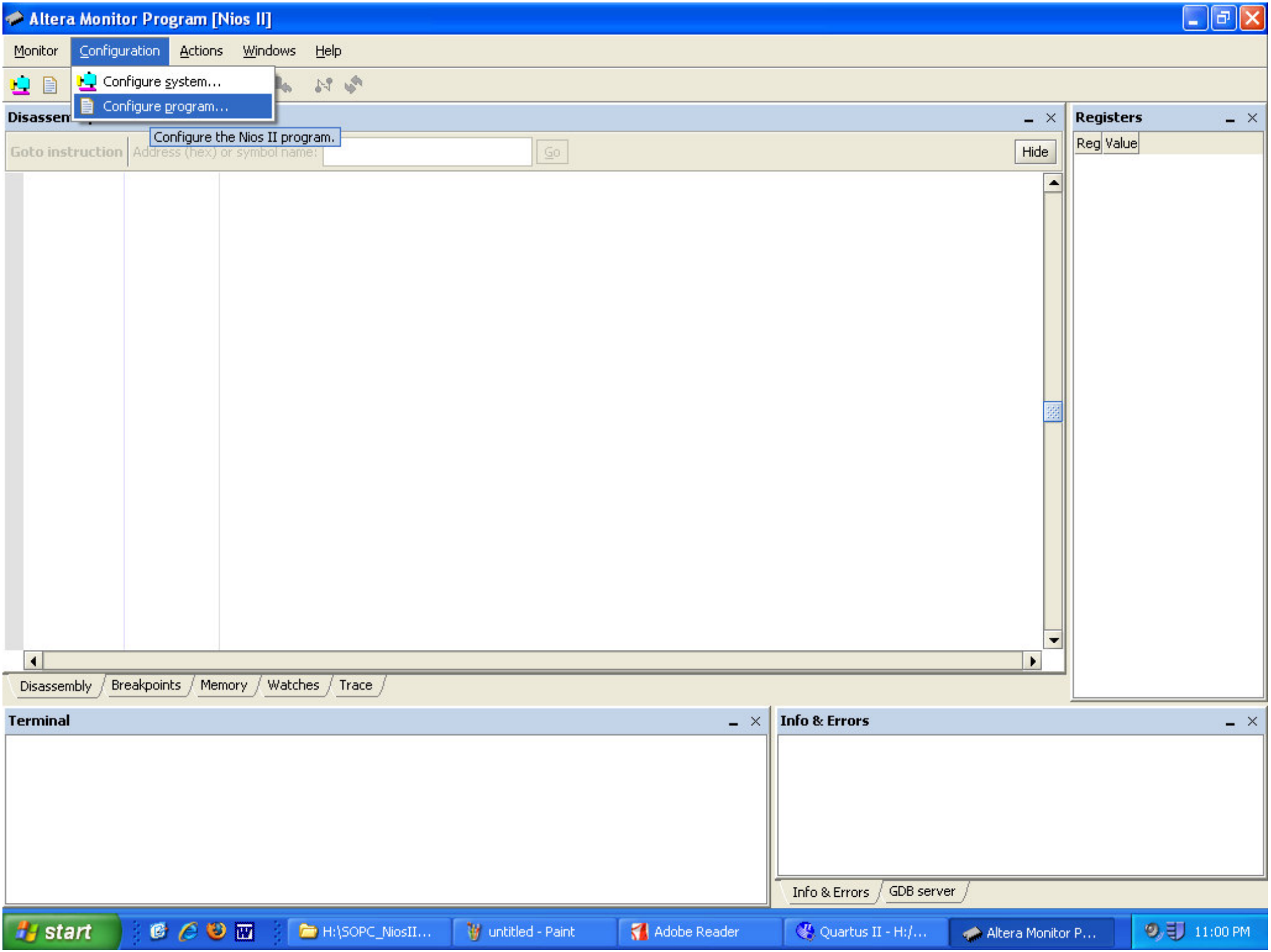
Nios II IDE program is used by professional circuit designer to test program on the Nios II processor.

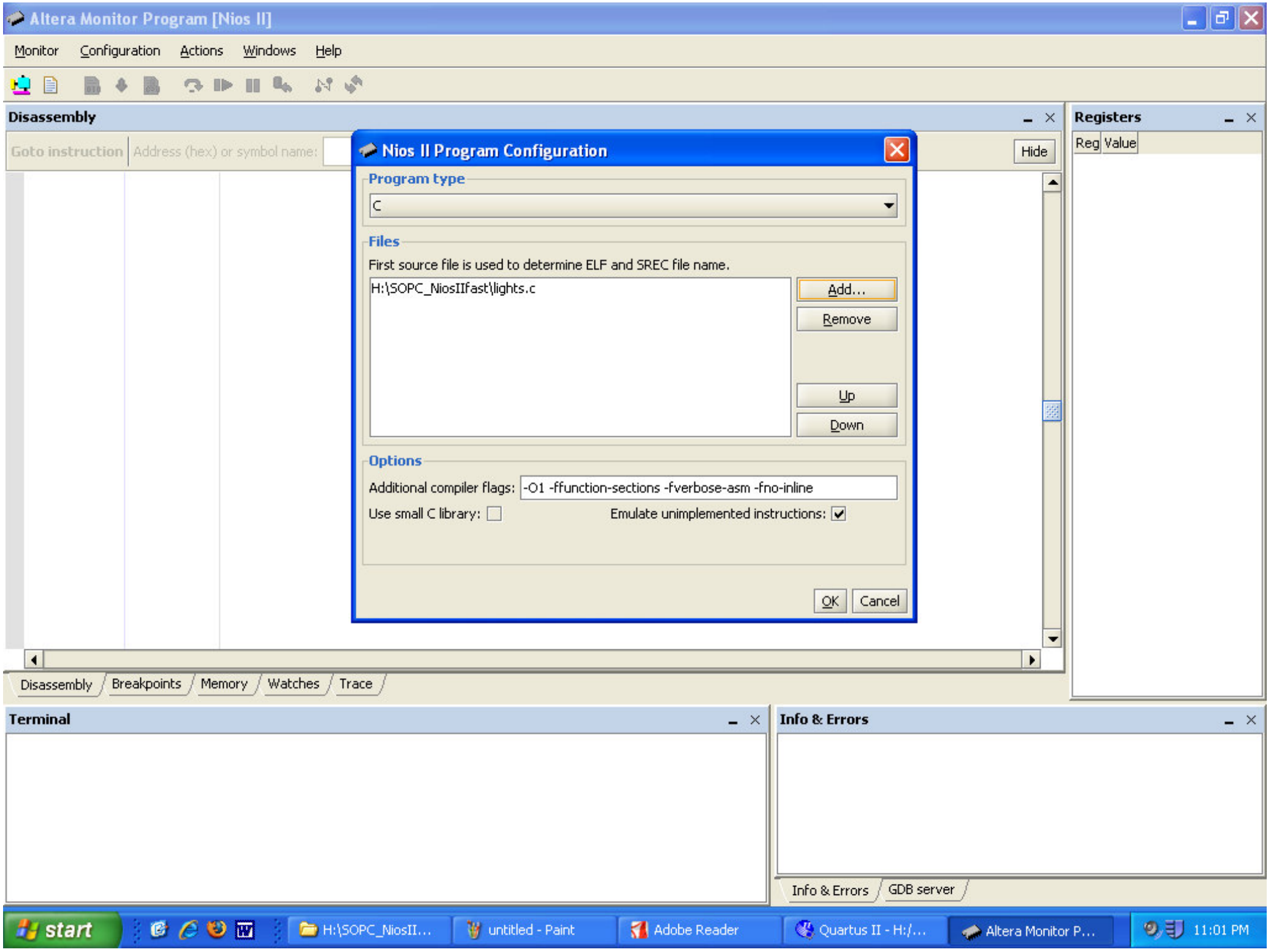

lights.c - Notepad
File Edit Format View Help
#define Switches (volatile char *) 0x00003000
#define LEDs (char *) 0x00003010
void main()
{
while(1)
*LEDs = *Switches;
}
start
H:\SOPC_N...
untitled - P...
Adobe Rea...
Quartus II ...
Altera Moni...
lights.c - N...
11:03 PM

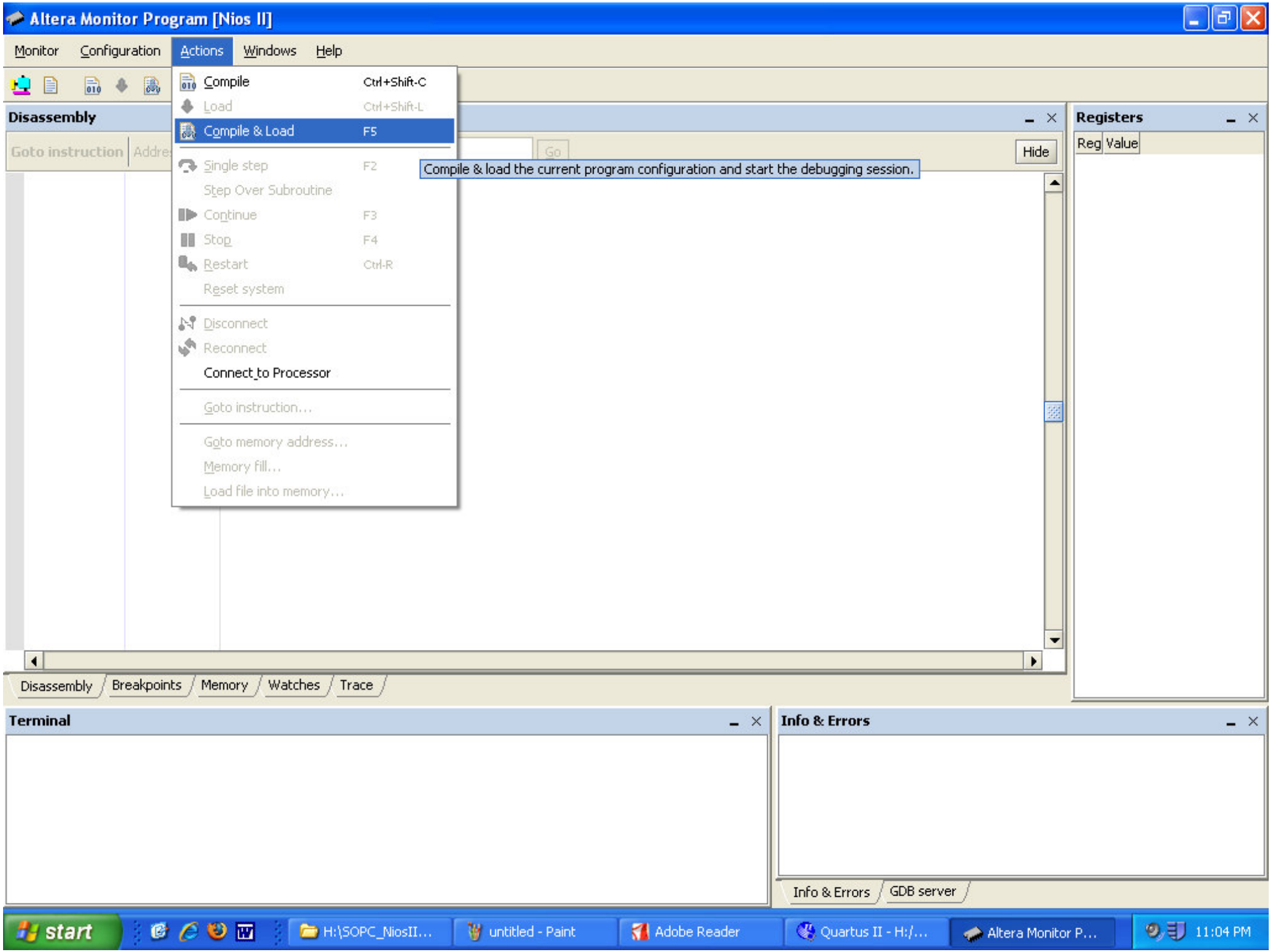

lights.c - Notepad
File Edit Format View Help
#define Switches (volatile char *) 0x00003000
#define LEDs (char *) 0x00003010
void main()
{
while(1)
*LEDs = *Switches;
}
Same memory addresses as "pio" and "pio_1"
start
H:\SOPC_N...
untitled - P...
Adobe Rea...
Quartus II ...
Altera Moni...
lights.c - N...
11:03 PM


Altera Monitor Program [Nios II]
Monitor
Configuration
Actions
Windows
Help
Configure system...
Configure program...
Configure the Nios II system.
Disassem
Goto instruction
Address (hex) or symbol name:
Go
Hide
Registers
Reg
Value
Disassembly
Breakpoints
Memory
Watches
Trace
Terminal
Info & Errors
Info & Errors
GDB server
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera Monitor P...
10:57 PM

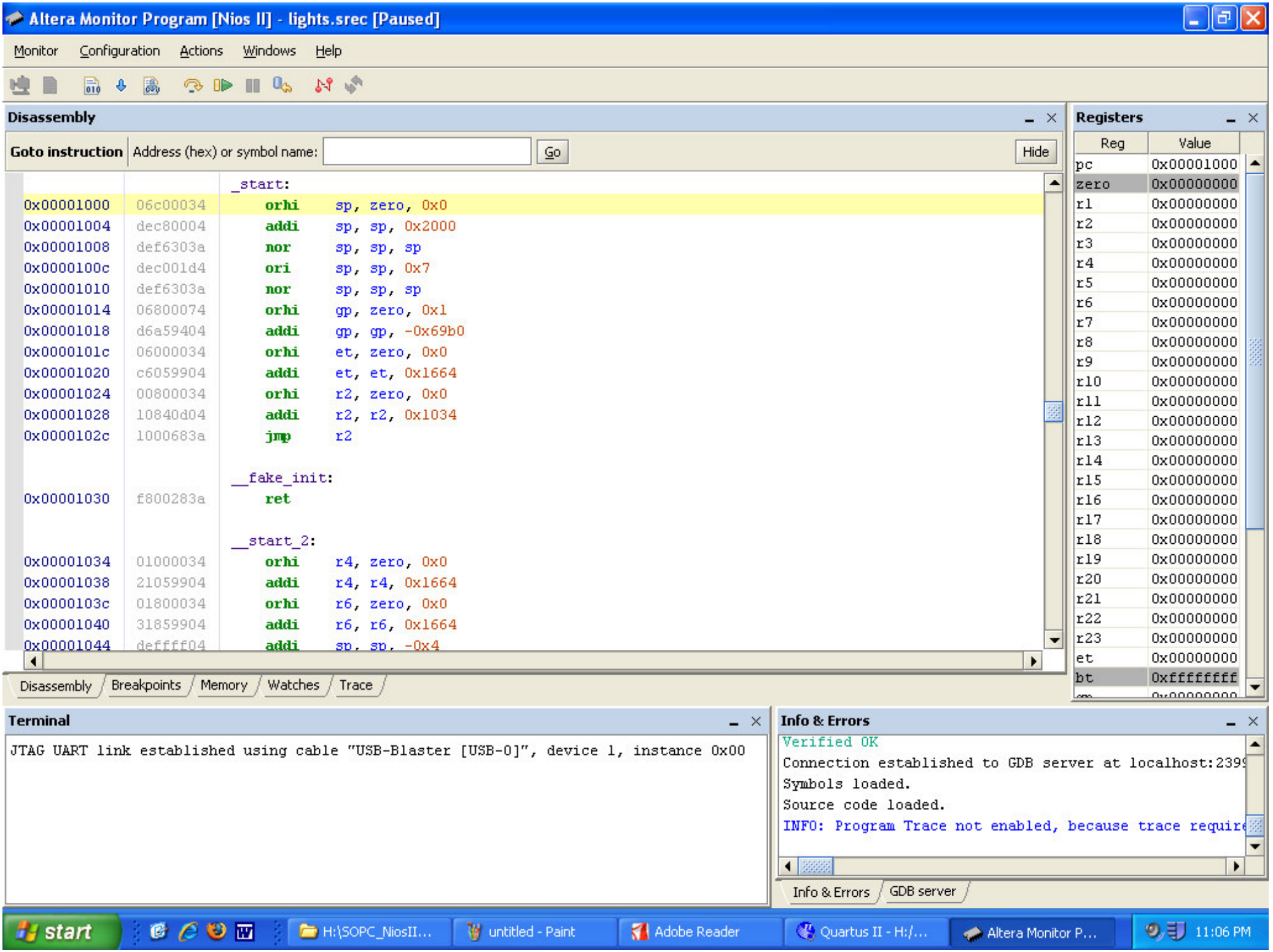

Altera Monitor Program [Nios II]
Monitor
Configuration
Actions
Windows
Help
Disassembly
Goto instruction
Address (hex) or symbol name:
Go
Hide
Registers
Reg
Value
Nios II System Configuration
Cable
USB-Blaster [USB-0]
Refresh
System description file (PTF)
H:\SOPC_NiosIIfast\nios_system.ptf
Browse...
Nios II Processor
cpu
.text section
Memory device:
onchip_mem/s1 (1000h - 1fffh)
Start offset in device (hex):
0
.data section
Memory device:
onchip_mem/s1 (1000h - 1fffh)
Start offset in device (hex):
0
Terminal device
jtag_uart
Refresh PTF File
OK
Cancel
Disassembly
Breakpoints
Memory
Watches
Trace
Terminal
Info & Errors
Info & Errors
GDB server
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera Monitor P...
10:59 PM


Altera Monitor Program [Nios II]
Monitor
Configuration
Actions
Windows
Help
Configure system...
Configure program...
Configure the Nios II program.
Disassem
Goto instruction
Address (hex) or symbol name:
Go
Hide
Registers
Reg
Value
Disassembly
Breakpoints
Memory
Watches
Trace
Terminal
Info & Errors
Info & Errors
GDB server
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera Monitor P...
11:00 PM


Altera Monitor Program [Nios II]
Monitor
Configuration
Actions
Windows
Help
Disassembly
Goto instruction
Address (hex) or symbol name:
Hide
Registers
Reg
Value
Nios II Program Configuration
Program type
C
Files
First source file is used to determine ELF and SREC file name.
H:\SOPC_NiosIIfast\lights.c
Add...
Remove
Up
Down
Options
Additional compiler flags:
-O1 -ffunction-sections -fverbose-asm -fno-inline
Use small C library:
Emulate unimplemented instructions:
OK
Cancel
Disassembly
Breakpoints
Memory
Watches
Trace
Terminal
Info & Errors
Info & Errors
GDB server
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera Monitor P...
11:01 PM


Altera Monitor Program [Nios II]
Monitor
Configuration
Actions
Windows
Help
Compile Ctrl+Shift-C
Load Ctrl+Shift-L
Compile & Load F5
Single step F2
Step Over Subroutine
Continue F3
Stop F4
Restart Ctrl-R
Reset system
Disconnect
Reconnect
Connect to Processor
Goto instruction...
Goto memory address...
Memory fill...
Load file into memory...
Compile & load the current program configuration and start the debugging session.
Disassembly
Goto instruction
Go
Hide
Registers
Reg
Value
Disassembly
Breakpoints
Memory
Watches
Trace
Terminal
Info & Errors
Info & Errors
GDB server
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera Monitor P...
11:04 PM

Remember to keep reset line HIGH


Altera Monitor Program [Nios II] - lights.srec [Paused]
Monitor Configuration Actions Windows Help
Disassembly
Goto instruction Address (hex) or symbol name: Go Hide
_start:
0x00001000 06c00034 orhi sp, zero, 0x0
0x00001004 dec80004 addi sp, sp, 0x2000
0x00001008 def6303a nor sp, sp, sp
0x0000100c dec001d4 ori sp, sp, 0x7
0x00001010 def6303a nor sp, sp, sp
0x00001014 06800074 orhi gp, zero, 0x1
0x00001018 d6a59404 addi gp, gp, -0x69b0
0x0000101c 06000034 orhi et, zero, 0x0
0x00001020 c6059904 addi et, et, 0x1664
0x00001024 00800034 orhi r2, zero, 0x0
0x00001028 10840d04 addi r2, r2, 0x1034
0x0000102c 1000683a jmp r2
__fake_init:
0x00001030 f800283a ret
__start_2:
0x00001034 01000034 orhi r4, zero, 0x0
0x00001038 21059904 addi r4, r4, 0x1664
0x0000103c 01800034 orhi r6, zero, 0x0
0x00001040 31859904 addi r6, r6, 0x1664
0x00001044 defffe04 addi sp, sp, -0x4
Disassembly Breakpoints Memory Watches Trace
Registers
Reg Value
pc 0x00001000
zero 0x00000000
r1 0x00000000
r2 0x00000000
r3 0x00000000
r4 0x00000000
r5 0x00000000
r6 0x00000000
r7 0x00000000
r8 0x00000000
r9 0x00000000
r10 0x00000000
r11 0x00000000
r12 0x00000000
r13 0x00000000
r14 0x00000000
r15 0x00000000
r16 0x00000000
r17 0x00000000
r18 0x00000000
r19 0x00000000
r20 0x00000000
r21 0x00000000
r22 0x00000000
r23 0x00000000
et 0x00000000
bt 0xffffffff
Terminal
JTAG UART link established using cable "USB-Blaster [USB-0]", device 1, instance 0x00
Info & Errors
Verified OK
Connection established to GDB server at localhost:239
Symbols loaded.
Source code loaded.
INFO: Program Trace not enabled, because trace require
Info & Errors GDB server
start
H:\SOPC_NiosII...
untitled - Paint
Adobe Reader
Quartus II - H:/...
Altera Monitor P...
11:06 PM