

ADC0820

8-Bit High Speed μ P Compatible A/D Converter with Track/Hold Function

General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 μ s conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/ μ s.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

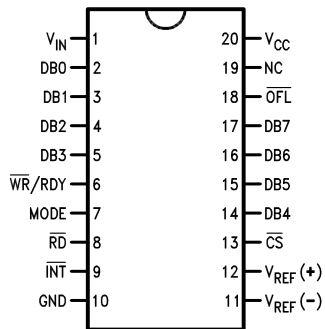
| | | |
|--------------------------|------------------------------|-------------------------------|
| ■ Resolution | | 8 Bits |
| ■ Conversion Time | 2.5 μ s Max (RD Mode) | |
| | 1.5 μ s Max (WR-RD Mode) | |
| ■ Low Power | | 75 mW Max |
| ■ Total Unadjusted Error | | $\pm 1/2$ LSB and ± 1 LSB |

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5 V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE output
- Logic inputs and outputs meet both MOS and T²L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP
- 20-pin molded chip carrier package
- 20-pin small outline package
- 20-pin shrink small outline package (SSOP)

Connection and Functional Diagrams

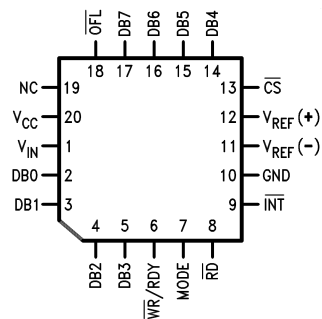
Dual-In-Line, Small Outline and SSOP Packages



Top View

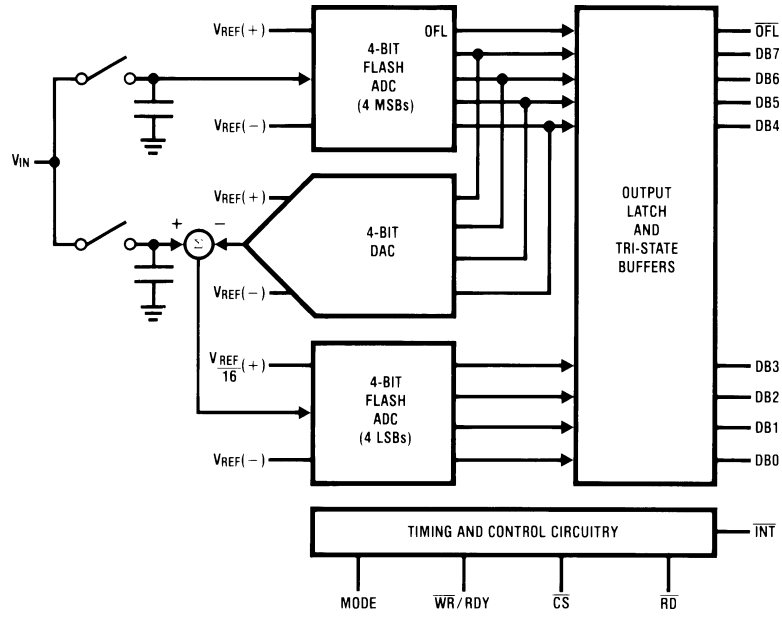
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Molded Chip Carrier Package



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Connection and Functional Diagrams (Continued)



00550102

FIGURE 1.

Ordering Information

| Part Number | Total Unadjusted Error | Package | Temperature Range |
|--|------------------------|--|--|
| ADC0820BCV ADC0820BCWM ADC0820BCN | $\pm 1/2$ LSB | V20A—Molded Chip Carrier M20B—Wide Body Small Outline N20A—Molded DIP | 0°C to +70°C 0°C to +70°C 0°C to +70°C |
| ADC0820CCJ ADC0820CCWM ADC0820CIWM ADC0820CCN | ± 1 LSB | J20A—Cerdip M20B—Wide Body Small Outline M20B—Wide Body Small Outline N20A—Molded DIP | -40°C to +85°C 0°C to +70°C -40°C to +85°C 0°C to +70°C |

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|-------------------------|
| Supply Voltage (V_{CC}) | 10V |
| Logic Control Inputs | -0.2V to V_{CC} +0.2V |
| Voltage at Other Inputs and Output | -0.2V to V_{CC} +0.2V |
| Storage Temperature Range | -65°C to +150°C |
| Package Dissipation at $T_A = 25^\circ\text{C}$ | 875 mW |
| Input Current at Any Pin (Note 5) | 1 mA |
| Package Input Current (Note 5) | 4 mA |
| ESD Susceptibility (Note 9) | 900V |
| Lead Temp. (Soldering, 10 sec.) | |
| Dual-In-Line Package (plastic) | 260°C |

| | |
|--------------------------------|-------|
| Dual-In-Line Package (ceramic) | 300°C |
| Surface Mount Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

Operating Ratings (Notes 1, 2)

| | |
|--------------------------|---------------------------------|
| Temperature Range | $T_{MIN} \leq T_A \leq T_{MAX}$ |
| ADC0820CCJ | -40°C $\leq T_A \leq$ +85°C |
| ADC0820CIWM | -40°C $\leq T_A \leq$ +85°C |
| ADC0820BCN, ADC0820CCN | 0°C $\leq T_A \leq$ 70°C |
| ADC0820BCV | 0°C $\leq T_A \leq$ 70°C |
| ADC0820BCWM, ADC0820CCWM | 0°C $\leq T_A \leq$ 70°C |
| V_{CC} Range | 4.5V to 8V |

Converter Characteristics

The following specifications apply for RD mode (pin 7=0), $V_{CC}=5\text{V}$, $V_{REF(+)}=5\text{V}$, and $V_{REF(-)}=GND$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; all other limits $T_A=T_j=25^\circ\text{C}$.

| Parameter | Conditions | ADC0820CCJ | | | ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820BCWM ADC0820CCWM, ADC0820CIWM | | | Limit Units |
|--------------------------------------|--|-----------------|--------------------------------|-----------------------------|---|---------------------------------|---|--------------------------------|
| | | Typ (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Typ (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | |
| Resolution | | | 8 | | | 8 | 8 | Bits |
| Total Unadjusted Error (Note 3) | ADC0820BCN, BCWM ADC0820CCJ ADC0820CCN, CCWM, CIWM ADC0820CCMSA | | ± 1 | | | $\pm 1/2$ ± 1 ± 1 | $\pm 1/2$ ± 1 ± 1 | LSB LSB LSB LSB |
| Minimum Reference Resistance | | 2.3 | 1.00 | | 2.3 | 1.2 | | k Ω |
| Maximum Reference Resistance | | 2.3 | 6 | | 2.3 | 5.3 | 6 | k Ω |
| Maximum $V_{REF(+)}$ Input Voltage | | | V_{CC} | | | V_{CC} | V_{CC} | V |
| Minimum $V_{REF(-)}$ Input Voltage | | | GND | | | GND | GND | V |
| Minimum $V_{REF(+)}$ Input Voltage | | | $V_{REF(-)}$ | | | $V_{REF(-)}$ | $V_{REF(-)}$ | V |
| Maximum $V_{REF(-)}$ Input Voltage | | | $V_{REF(+)}$ | | | $V_{REF(+)}$ | $V_{REF(+)}$ | V |
| Maximum V_{IN} Input Voltage | | | $V_{CC}+0.1$ | | | $V_{CC}+0.1$ | $V_{CC}+0.1$ | V |
| Minimum V_{IN} Input Voltage | | | GND-0.1 | | | GND-0.1 | GND-0.1 | V |
| Maximum Analog Input Leakage Current | $\overline{CS} = V_{CC}$ $V_{IN} = V_{CC}$ $V_{IN} = GND$ | | 3 -3 | | | 0.3 -0.3 | 3 -3 | μA μA |
| Power Supply Sensitivity | $V_{CC} = 5\text{V} \pm 5\%$ | $\pm 1/16$ | $\pm 1/4$ | | $\pm 1/16$ | $\pm 1/4$ | $\pm 1/4$ | LSB |

DC Electrical Characteristics

The following specifications apply for $V_{CC}=5V$, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; all other limits $T_A=T_J=25^\circ C$.

| Parameter | Conditions | | ADC0820CCJ | | | ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820BCWM ADC0820CCWM, ADC0820CIWM | | | Limit Units |
|--|--|---|-----------------|-----------------------------|-----------------------------|---|-----------------------------|-----------------------------|-------------|
| | | | Typ (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Typ (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | |
| $V_{IN(1)}$, Logical "1" Input Voltage | $V_{CC}=5.25V$ | \overline{CS} , \overline{WR} , \overline{RD} | | 2.0 | | | 2.0 | 2.0 | V |
| | | Mode | | 3.5 | | | 3.5 | 3.5 | V |
| $V_{IN(0)}$, Logical "0" Input Voltage | $V_{CC}=4.75V$ | \overline{CS} , \overline{WR} , \overline{RD} | | 0.8 | | | 0.8 | 0.8 | V |
| | | Mode | | 1.5 | | | 1.5 | 1.5 | V |
| $I_{IN(1)}$, Logical "1" Input Current | $V_{IN(1)}=5V$; \overline{CS} , \overline{RD} | | 0.005 | 1 | | 0.005 | | 1 | μA |
| | | $V_{IN(1)}=5V$; \overline{WR} | 0.1 | 3 | | 0.1 | 0.3 | 3 | μA |
| | | $V_{IN(1)}=5V$; Mode | 50 | 200 | | 50 | 170 | 200 | μA |
| $I_{IN(0)}$, Logical "0" Input Current | $V_{IN(0)}=0V$; \overline{CS} , \overline{RD} , \overline{WR} , Mode | | -0.005 | -1 | | -0.005 | | -1 | μA |
| $V_{OUT(1)}$, Logical "1" Output Voltage | $V_{CC}=4.75V$, $I_{OUT}=-360 \mu A$; $DB0-DB7$, \overline{OFL} , \overline{INT} | | | 2.4 | | | 2.8 | 2.4 | V |
| | | $V_{CC}=4.75V$, $I_{OUT}=-10 \mu A$; $DB0-DB7$, \overline{OFL} , \overline{INT} | | | 4.5 | | | 4.6 | 4.5 |
| $V_{OUT(0)}$, Logical "0" Output Voltage | $V_{CC}=4.75V$, $I_{OUT}=1.6 mA$; $DB0-DB7$, \overline{OFL} , \overline{INT} , RDY | | | 0.4 | | | 0.34 | 0.4 | V |
| I_{OUT} , TRI-STATE Output Current | $V_{OUT}=5V$; $DB0-DB7$, RDY $V_{OUT}=0V$; $DB0-DB7$, RDY | | 0.1 | 3 | | 0.1 | 0.3 | 3 | μA |
| | | | -0.1 | -3 | | -0.1 | -0.3 | -3 | μA |
| I_{SOURCE} , Output Source Current | $V_{OUT}=0V$; $DB0-DB7$, \overline{OFL} , \overline{INT} | | -12 | -6 | | -12 | -7.2 | -6 | mA |
| | | | -9 | -4.0 | | -9 | -5.3 | -4.0 | mA |
| I_{SINK} , Output Sink Current | $V_{OUT}=5V$; $DB0-DB7$, \overline{OFL} , \overline{INT} , RDY | | 14 | 7 | | 14 | 8.4 | 7 | mA |
| I_{CC} , Supply Current | $\overline{CS} = \overline{WR} = \overline{RD} = 0$ | | 7.5 | 15 | | 7.5 | 13 | 15 | mA |

AC Electrical Characteristics

The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20 ns$, $V_{REF(+)}=5V$, $V_{REF(-)}=0V$ and $T_A=25^\circ C$ unless otherwise specified.

| Parameter | Conditions | Typ (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Units |
|--|---|--|-----------------------------|-----------------------------|---------|
| t_{CRD} , Conversion Time for RD Mode | Pin 7 = 0, <i>Figure 2</i> | 1.6 | | 2.5 | μs |
| t_{ACC0} , Access Time (Delay from Falling Edge of \overline{RD} to Output Valid) | Pin 7 = 0, <i>Figure 2</i> | | $t_{CRD}+20$ | $t_{CRD}+50$ | ns |
| t_{CWR-RD} , Conversion Time for WR-RD Mode | Pin 7 = V_{CC} ; $t_{WR} = 600 ns$, $t_{RD}=600 ns$; <i>Figures 3, 4</i> | | | 1.52 | μs |
| t_{WR} , Write Time | Min | Pin 7 = V_{CC} ; <i>Figures 3, 4</i> (Note 4) See Graph | | 600 | ns |
| | | | Max | 50 | μs |
| t_{RD} , Read Time | Min | Pin 7 = V_{CC} ; <i>Figures 3, 4</i> (Note 4) See Graph | | 600 | ns |
| t_{ACC1} , Access Time (Delay from Falling Edge of \overline{RD} to Output Valid) | $C_L=15 pF$ | Pin 7 = V_{CC} , $t_{RD}<t_i$; <i>Figure 3</i> | | 190 | ns |
| | | | $C_L=100 pF$ | 210 | 320 |

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns, $V_{REF(+)}=5V$, $V_{REF(-)}=0V$ and $T_A=25^\circ C$ unless otherwise specified.

| Parameter | Conditions | Typ (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Units |
|---|---|-----------------|-----------------------------|-----------------------------|------------|
| t_{ACC2} , Access Time (Delay from Falling Edge of \overline{RD} to Output Valid) | Pin 7 = V_{CC} , $t_{RD} > t_i$; <i>Figure 4</i> $C_L=15$ pF | 70 | | 120 | ns |
| | $C_L=100$ pF | 90 | | 150 | ns |
| t_{ACC3} , Access Time (Delay from Rising Edge of RDY to Output Valid) | $R_{PULLUP} = 1k$ and $C_L = 15$ pF | 30 | | | ns |
| t_i , Internal Comparison Time | Pin 7= V_{CC} ; <i>Figures 4, 5</i> $C_L=50$ pF | 800 | | 1300 | ns |
| t_{1H} , t_{0H} , TRI-STATE Control (Delay from Rising Edge of \overline{RD} to Hi-Z State) | $R_L=1k$, $C_L=10$ pF | 100 | | 200 | ns |
| t_{INTL} , Delay from Rising Edge of \overline{WR} to Falling Edge of \overline{INT} | Pin 7 = V_{CC} , $C_L= 50$ pF $t_{RD} > t_i$; <i>Figure 4</i> $t_{RD} < t_i$; <i>Figure 3</i> | | | t_i | ns |
| | | $t_{RD}+200$ | | $t_{RD}+290$ | ns |
| t_{INTH} , Delay from Rising Edge of \overline{RD} to Rising Edge of \overline{INT} | <i>Figures 2, 3, 4</i> $C_L=50$ pF | 125 | | 225 | ns |
| t_{INTHWR} , Delay from Rising Edge of \overline{WR} to Rising Edge of \overline{INT} | <i>Figure 5</i> , $C_L=50$ pF | 175 | | 270 | ns |
| t_{RDY} , Delay from \overline{CS} to RDY | <i>Figure 2</i> , $C_L=50$ pF, Pin 7 =0 | 50 | | 100 | ns |
| t_{ID} , Delay from \overline{INT} to Output Valid | <i>Figure 5</i> | 20 | | 50 | ns |
| t_{RI} , Delay from \overline{RD} to \overline{INT} | Pin 7= V_{CC} , $t_{RD} < t_i$ <i>Figure 3</i> | 200 | | 290 | ns |
| t_P , Delay from End of Conversion to Next Conversion | <i>Figures 2, 3, 4, 5</i> (Note 4) See Graph | | | 500 | ns |
| Slew Rate, Tracking | | 0.1 | | | V/ μ s |
| C_{VIN} , Analog Input Capacitance | | 45 | | | pF |
| C_{OUT} , Logic Output Capacitance | | 5 | | | pF |
| C_{IN} , Logic Input Capacitance | | 5 | | | pF |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs. t_{WR} and Accuracy vs. t_{RD} graphs.

Note 5: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.

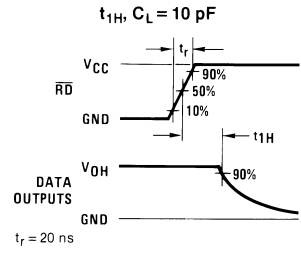
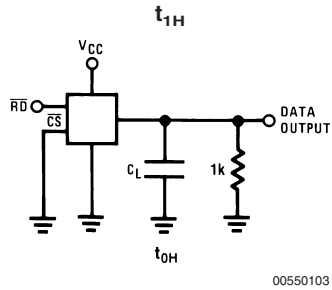
Note 6: Typicals are at $25^\circ C$ and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

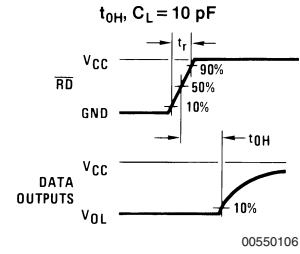
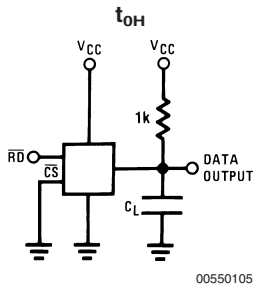
Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 9: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

TRI-STATE Test Circuits and Waveforms

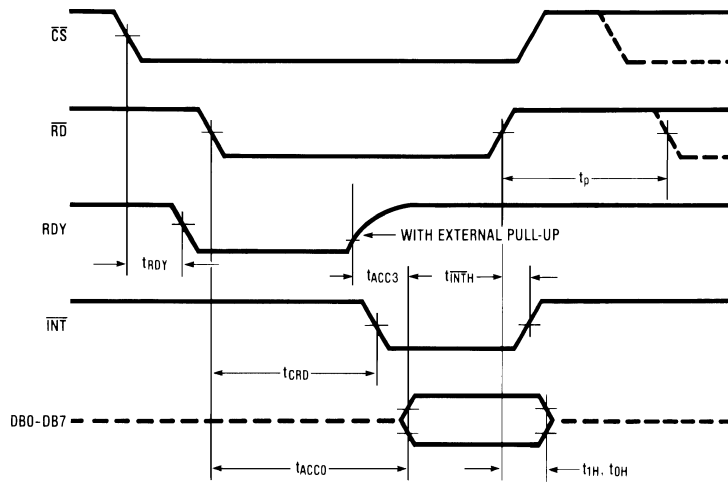


$t_r=20\text{ ns}$



$t_r=20\text{ ns}$

Timing Diagrams



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Note: On power-up the state of $\overline{\text{INT}}$ can be high or low.

FIGURE 2. RD Mode (Pin 7 is Low)

Timing Diagrams (Continued)

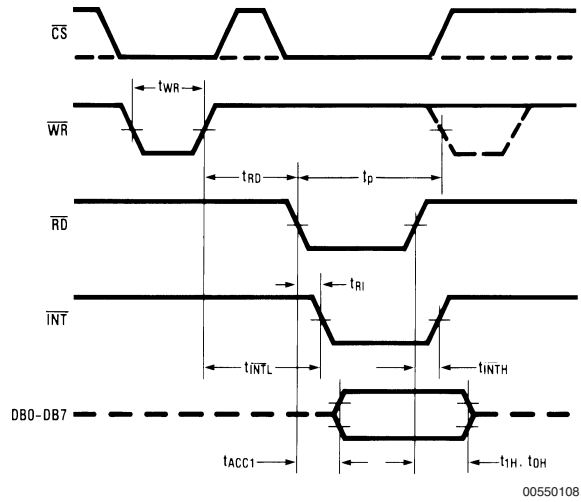


FIGURE 3. WR-RD Mode (Pin 7 is High and $t_{RD} < t_i$)

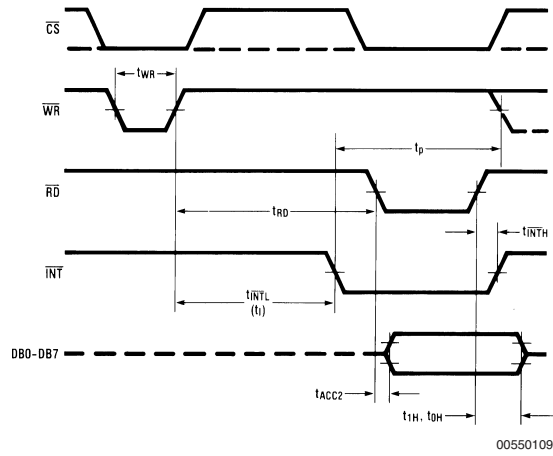


FIGURE 4. WR-RD Mode (Pin 7 is High and $t_{RD} > t_i$)

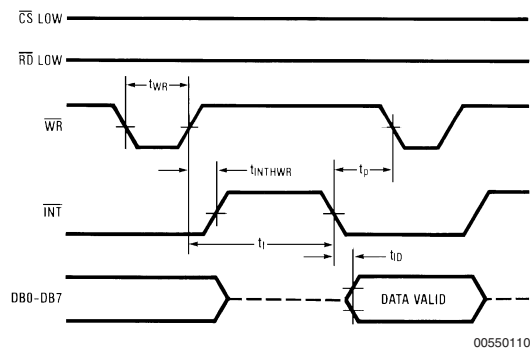
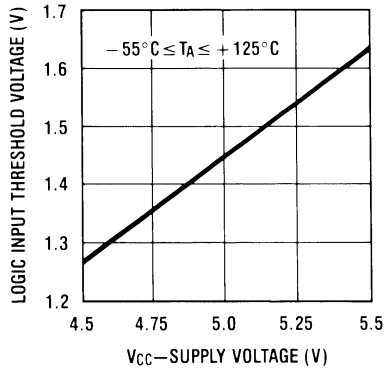


FIGURE 5. WR-RD Mode (Pin 7 is High) Stand-Alone Operation

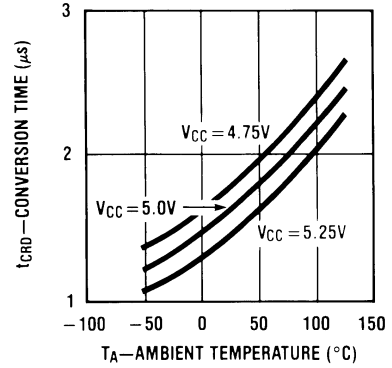
Typical Performance Characteristics

Logic Input Threshold Voltage vs. Supply Voltage



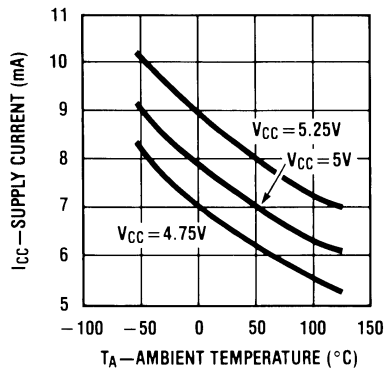
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Conversion Time (RD Mode) vs. Temperature



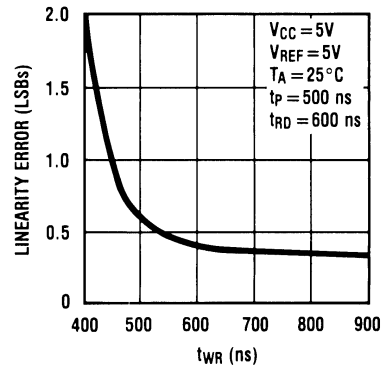
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Power Supply Current vs. Temperature (not including reference ladder)



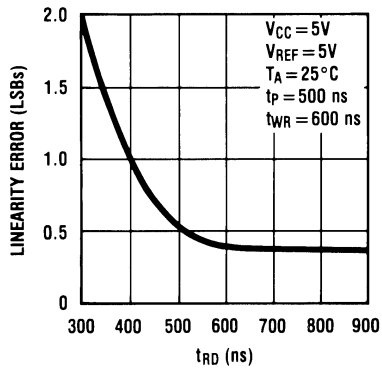
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Accuracy vs. tWR



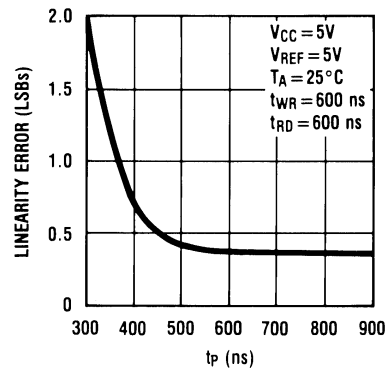
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Accuracy vs. tRD



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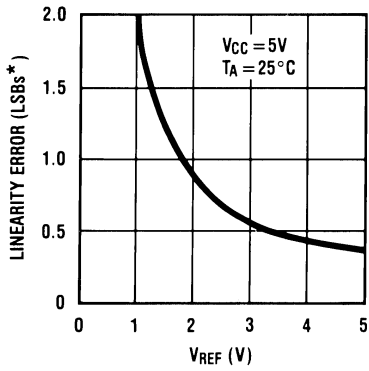
Accuracy vs. tp



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Typical Performance Characteristics (Continued)

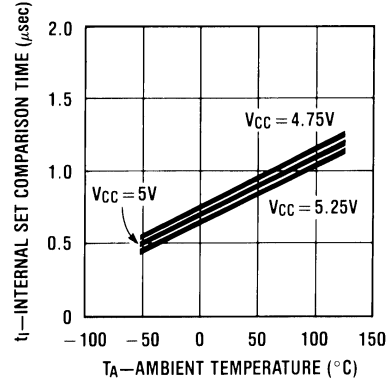
Accuracy vs. V_{REF} [$V_{REF}=V_{REF(+)}-V_{REF(-)}$]



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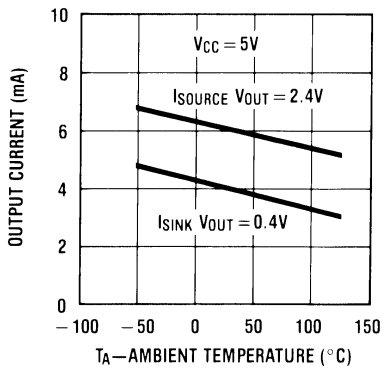
$$*1 \text{ LSB} = \frac{V_{REF}}{256}$$

t_{η} , Internal Time Delay vs. Temperature



00550141

Output Current vs. Temperature



00550142

| Description of Pin Functions | | Pin Name | Function |
|------------------------------|---|----------|---|
| Pin Name | Function | | |
| 1 | V_{IN} Analog input; range = $GND \leq V_{IN} \leq V_{CC}$ | 9 | \overline{INT} WR-RD Mode \overline{INT} going low indicates that the conversion is completed and the data result is in the output latch. \overline{INT} will go low, ~800 ns (the preset internal time out, t_I) after the rising edge of \overline{WR} (see <i>Figure 4</i>); or \overline{INT} will go low after the falling edge of \overline{RD} , if \overline{RD} goes low prior to the 800 ns time out (see <i>Figure 3</i>). \overline{INT} is reset by the rising edge of \overline{RD} or \overline{CS} (see <i>Figures 3, 4</i>). RD Mode \overline{INT} going low indicates that the conversion is completed and the data result is in the output latch. \overline{INT} is reset by the rising edge of \overline{RD} or \overline{CS} (see <i>Figure 2</i>). |
| 2 | DB0 TRI-STATE data output—bit 0 (LSB) | 10 | GND Ground |
| 3 | DB1 TRI-STATE data output—bit 1 | 11 | $V_{REF(-)}$ The bottom of resistor ladder, voltage range: $GND \leq V_{REF(-)} \leq V_{REF(+)}$ (Note 5) |
| 4 | DB2 TRI-STATE data output—bit 2 | 12 | $V_{REF(+)}$ The top of resistor ladder, voltage range: $V_{REF(-)} \leq V_{REF(+)} \leq V_{CC}$ (Note 5) |
| 5 | DB3 TRI-STATE data output—bit 3 | 13 | \overline{CS} \overline{CS} must be low in order for the \overline{RD} or \overline{WR} to be recognized by the converter. |
| 6 | \overline{WR} WR-RD Mode \overline{WR} : With \overline{CS} low, the conversion is started on the falling edge of \overline{WR} . Approximately 800 ns (the preset internal time out, t_I) after the \overline{WR} rising edge, the result of the conversion will be strobed into the output latch, provided that \overline{RD} does not occur prior to this time out (see <i>Figures 3, 4</i>). RD Mode RDY : This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of \overline{CS} ; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see <i>Figure 2</i>). Mode : Mode selection input—it is internally tied to GND through a 50 μ A current source. RD Mode : When mode is low WR-RD Mode : When mode is high | 14 | DB4 TRI-STATE data output—bit 4 |
| 7 | Mode | 15 | DB5 TRI-STATE data output—bit 5 |
| 8 | \overline{RD} WR-RD Mode With \overline{CS} low, the TRI-STATE data outputs (DB0-DB7) will be activated when \overline{RD} goes low (see <i>Figure 5</i>). \overline{RD} can also be used to increase the speed of the converter by reading data prior to the preset internal time out (t_I , ~800 ns). If this is done, the data result transferred to output latch is latched after the falling edge of the \overline{RD} (see <i>Figures 3, 4</i>). RD Mode With \overline{CS} low, the conversion will start with \overline{RD} going low, also \overline{RD} will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and \overline{INT} going low indicates the completion of the conversion (see <i>Figure 2</i>). | 16 | DB6 TRI-STATE data output—bit 6 |
| | | 17 | DB7 TRI-STATE data output—bit 7 (MSB) |
| | | 18 | \overline{OFL} Overflow output—If the analog input is higher than the $V_{REF(+)}$, \overline{OFL} will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit). This output is always active and does not go into TRI-STATE as DB0–DB7 do. |
| | | 19 | NC No connection |
| | | 20 | V_{CC} Power supply voltage |

1.0 Functional Description

1.1 GENERAL OPERATION

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (*Figure 1*). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder

1.0 Functional Description (Continued)

which most closely approximates the analog input. In addition, the “sampled-data” comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

1.2 THE SAMPLED-DATA COMPARATOR

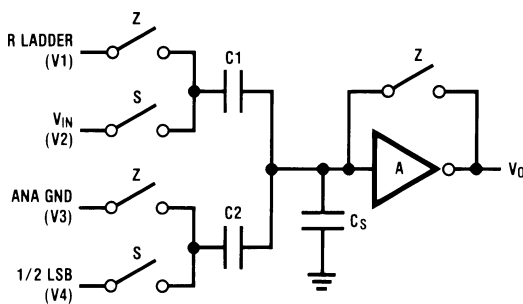
Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively coupled input (Figures 6, 7). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter’s input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter’s feedback switch (Figure 6) are closed. In this interval, C is charged to the connected input (V1) less the inverter’s bias voltage (V_B, approximately 1.2V). In the second cycle (Figure 7), these two switches are opened and the other (V2) input’s switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter’s open loop gain. The inverter’s input (V_B′) becomes

$$V_B - (V_1 - V_2) \frac{C}{C + C_S}$$

and the output will go high or low depending on the sign of V_B′ - V_B.

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (Figure 8), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor and opening all of the other switches (S switches). The change in voltage at the inverter’s input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

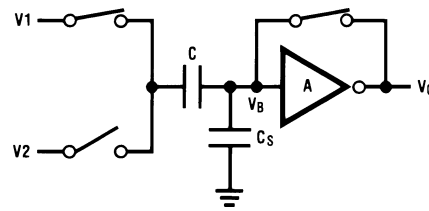


00550114

FIGURE 8. ADC0820 Comparator (from MS Flash ADC)

1.3 ARCHITECTURE

In the ADC0820, one bank of 15 comparators is used in each 4-bit flash A/D converter (Figure 12). The MS (most significant) flash ADC also has one additional comparator to detect

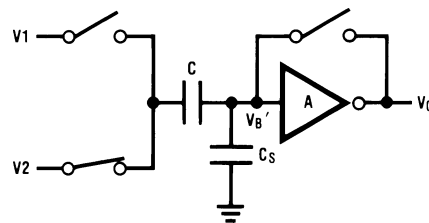


00550112

- V_O = V_B
- V on C = V₁ - V_B
- C_S = stray input node capacitor
- V_B = inverter input bias voltage

Zeroing Phase

FIGURE 6. Sampled-Data Comparator



00550113

- V_B′ - V_B = (V₂ - V₁) $\frac{C}{C + C_S}$
- V_O′ = $\frac{-A}{C + C_S} [CV_2 - CV_1]$
- V_O′ is dependent on V₂ - V₁

Compare Phase

FIGURE 7. Sampled-Data Comparator

$$V_O = \frac{-A}{C_1 + C_2 + C_S} [C_1(V_2 - V_1) + C_2(V_4 - V_3)]$$

$$= \frac{-A}{C_1 + C_2 + C_S} [\Delta Q_{C1} + \Delta Q_{C2}]$$

00550145

input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.

When a typical conversion is started, the \overline{WR} line is brought low. At this instant the MS comparators go from zeroing to

1.0 Functional Description (Continued)

comparison mode (Figure 11). When \overline{WR} is returned high after at least 600 ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600 ns later, the \overline{RD} line may be pulled low to latch the lower 4 data bits and finish the 8-bit conversion. When \overline{RD} goes low, the flash A/Ds change state once again in preparation for the next conversion.

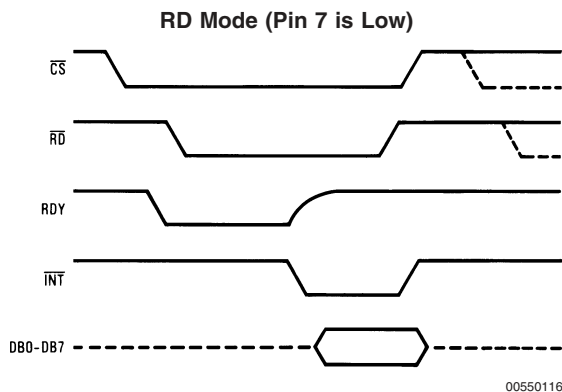
Figure 11 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while \overline{WR} is low. In RD mode, sampling occurs during the first 800 ns of \overline{RD} . Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant (Section 2.4), despite the fact that two separate 4-bit conversions are being done. More specifically, when \overline{WR} is low the MS flash is in compare mode (connected to V_{IN}), and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

1.4 DIGITAL INTERFACE

The ADC0820 has two basic interface modes which are selected by strapping the MODE pin high or low.

RD Mode

With the MODE pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling \overline{RD} low until output data appears. An \overline{INT} line is provided which goes low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.



When in RD mode, the comparator phases are internally triggered. At the falling edge of \overline{RD} , the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800 ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800 ns, the lower 4 bits are recovered.

WR then RD Mode

With the MODE pin tied high, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the \overline{WR} input; however, there are two options for reading the output

data which relate to interface timing. If an interrupt driven scheme is desired, the user can wait for \overline{INT} to go low before reading the conversion result (Figure 10). \overline{INT} will typically go low 800 ns after \overline{WR} 's rising edge. However, if a shorter conversion time is desired, the processor need not wait for \overline{INT} and can exercise a read after only 600 ns (Figure 9). If this is done, \overline{INT} will immediately go low and data will appear at the outputs.

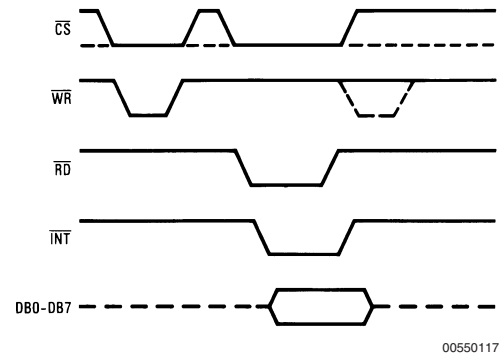


FIGURE 9. WR-RD Mode (Pin 7 is High and $t_{RD} < t_t$)

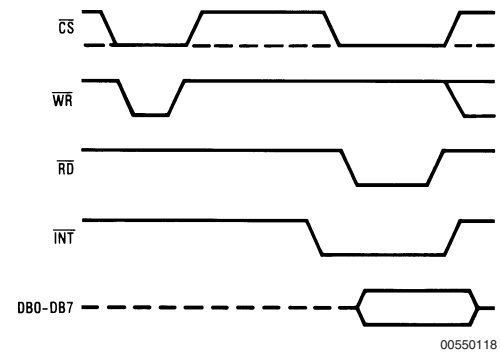
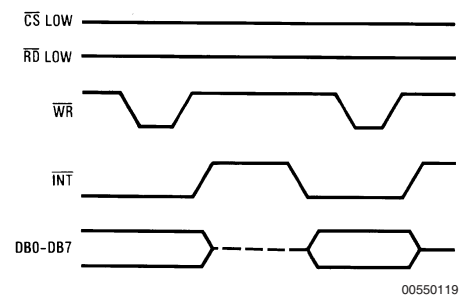


FIGURE 10. WR-RD Mode (Pin 7 is High and $t_{RD} > t_t$)

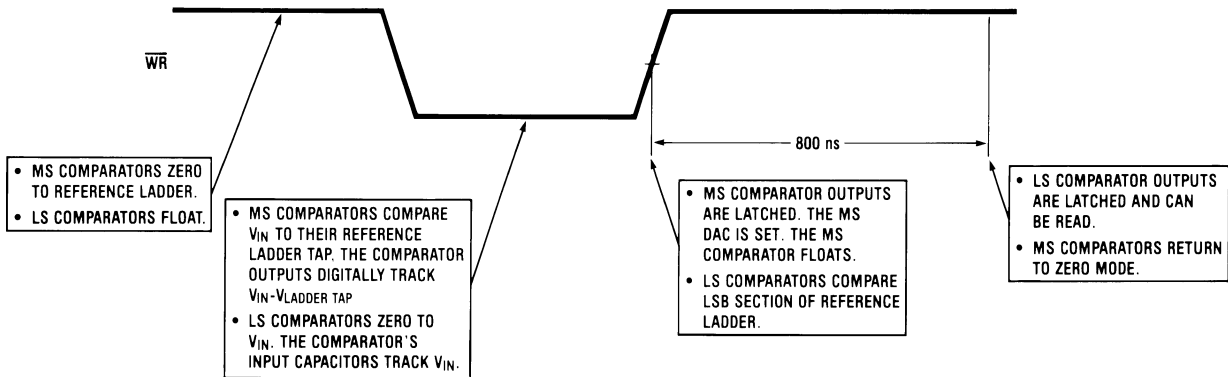
Stand-Alone

For stand-alone operation in WR-RD mode, \overline{CS} and \overline{RD} can be tied low and a conversion can be started with \overline{WR} . Data will be valid approximately 800 ns following \overline{WR} 's rising edge.

WR-RD Mode (Pin 7 is High) Stand-Alone Operation



1.0 Functional Description (Continued)



00550120

Note: MS means most significant
LS means least significant

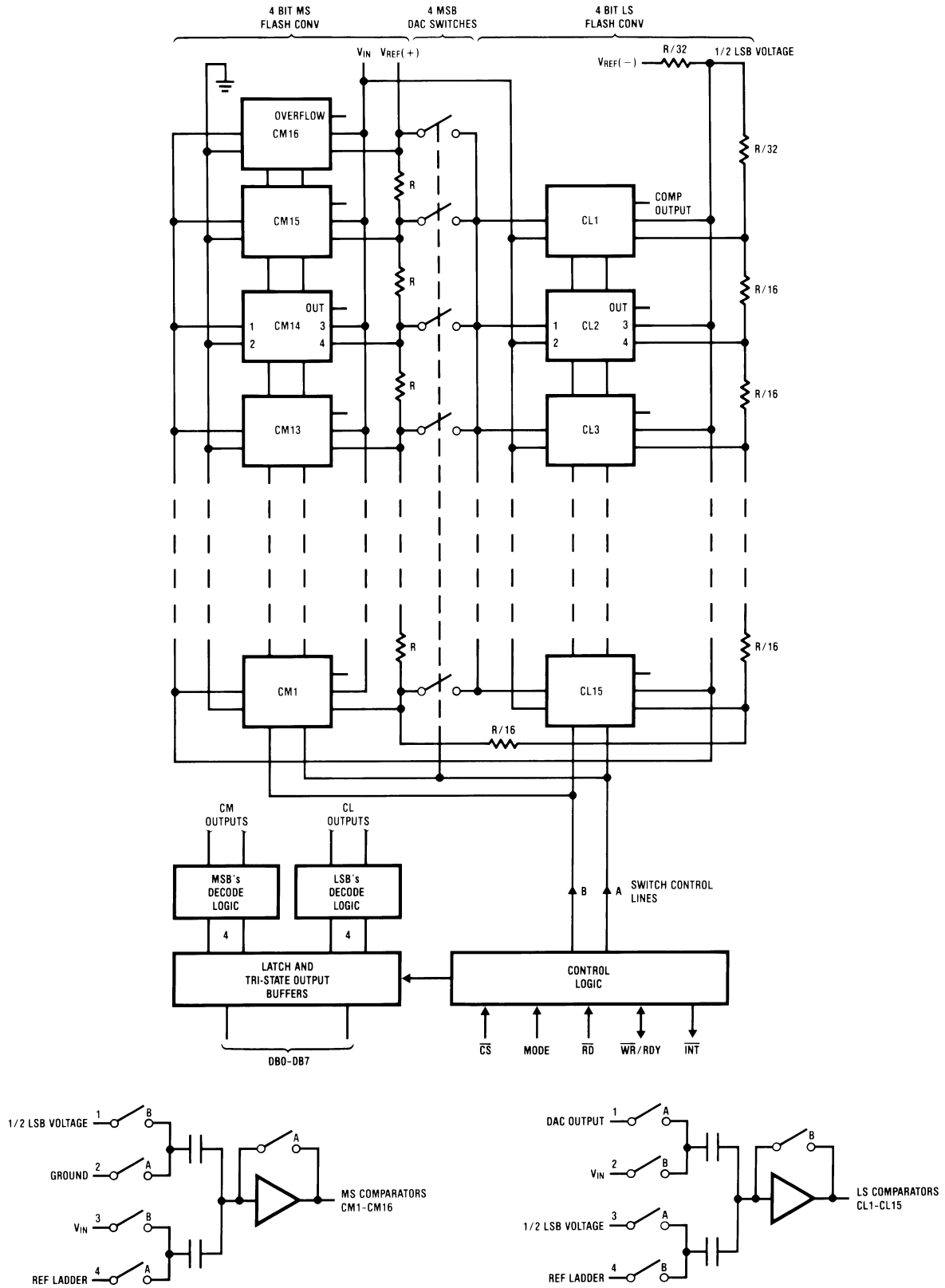
FIGURE 11. Operating Sequence (WR-RD Mode)

OTHER INTERFACE CONSIDERATIONS

In order to maintain conversion accuracy, \overline{WR} has a maximum width spec of 50 μ s. When the MS flash ADC's sampled-data comparators (Section 1.2) are in comparison mode (\overline{WR} is low), the input capacitors (C, Figure 8) must hold their charge. Switch leakage and inverter bias current can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion (Section 1.3), a new conversion cannot be started until this phase is complete. The minimum spec for this time (t_p , Figures 2, 3, 4, 5) is 500 ns.

Detailed Block Diagram



00550115

FIGURE 12.

2.0 Analog Considerations

2.1 REFERENCE AND INPUT

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN(+)}$ and $V_{IN(-)}$. By reducing V_{REF} ($V_{REF}=V_{REF(+)}-V_{REF(-)}$) to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF}=2V$ then $1\text{ LSB}=7.8\text{ mV}$). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF(-)}$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. *Figure 13* shows some of the configurations that are possible.

2.2 INPUT CURRENT

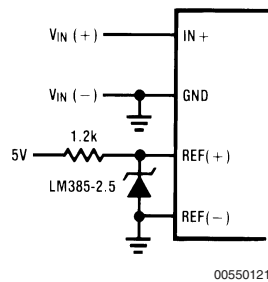
Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820 is shown in *Figure 14*. When a conversion starts (\overline{WR} low, WR-RD mode), all input switches close, connecting V_{IN} to thirty-one 1 pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase (Section 1.3). In other words, the LS ADC uses V_{IN} as its zero-phase input.

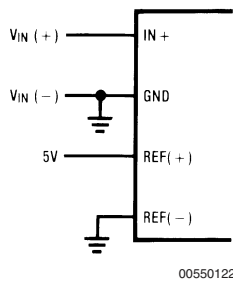
The input capacitors must charge to the input voltage through the on resistance of the analog switches (about $5\text{ k}\Omega$ to $10\text{ k}\Omega$). In addition, about 12 pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in *Figure 15*. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800 ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that \overline{WR} is low. Since other factors force this time to be at least 600 ns , input time constants of 100 ns can be accommodated without special consideration. Typical total input capacitance values of 45 pF allow R_S to be $1.5\text{ k}\Omega$ without lengthening \overline{WR} to give V_{IN} more time to settle.

External Reference 2.5V Full-Scale



Power Supply as Reference



Input Not Referred to GND

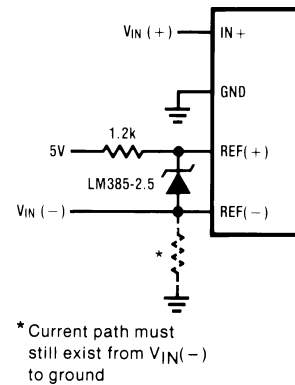


FIGURE 13. Analog Input Options

2.0 Analog Considerations (Continued)

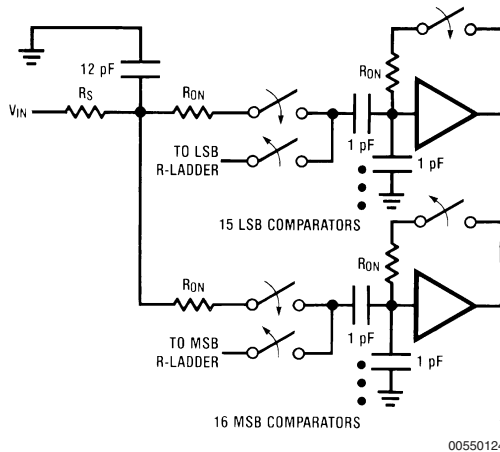


FIGURE 14.

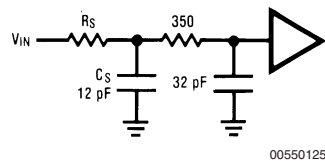


FIGURE 15.

2.3 INPUT FILTERING

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN} , will not degrade the A/D's performance in most cases. In effect the ADC0820 does not "look" at the input when these transients

occur. The comparators' outputs are not latched while \overline{WR} is low, so at least 600 ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal.

2.4 INHERENT SAMPLE-HOLD

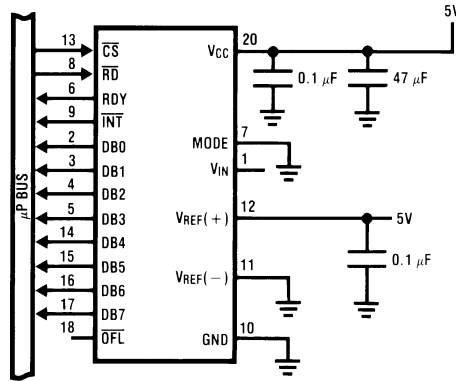
Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least $\frac{1}{2}$ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled-data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5 μ s, the time through which V_{IN} must be $\frac{1}{2}$ LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when \overline{WR} is low (Sections 1.3 and 2.2). Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100 ns after the rising edge of \overline{WR} (100 ns due to internal logic prop delay) will be the measured value.

Input signals with slew rates typically below 100 mV/ μ s can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1 μ s would still not be able to measure a 5V 1 kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7 kHz waveforms.

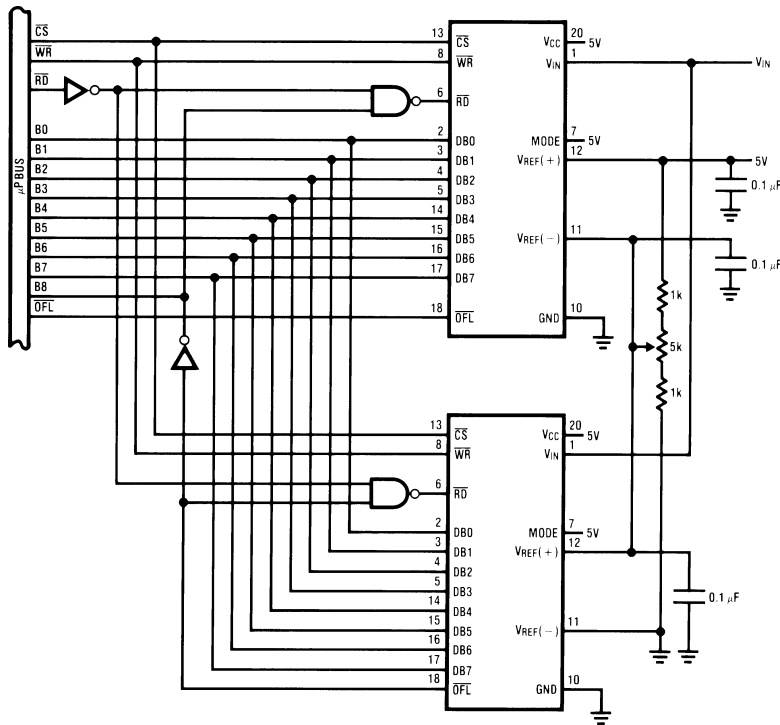
3.0 Typical Applications

8-Bit Resolution Configuration



00550126

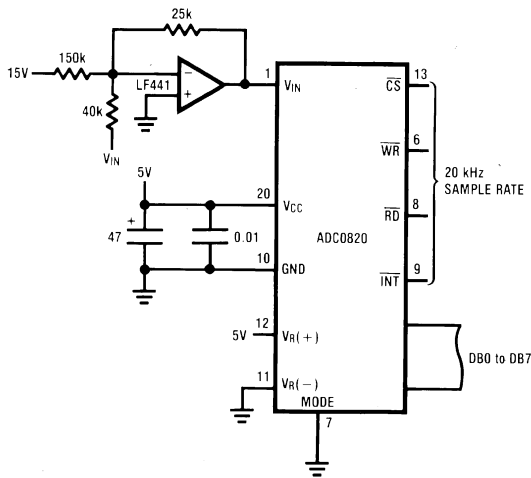
9-Bit Resolution Configuration



00550127

3.0 Typical Applications (Continued)

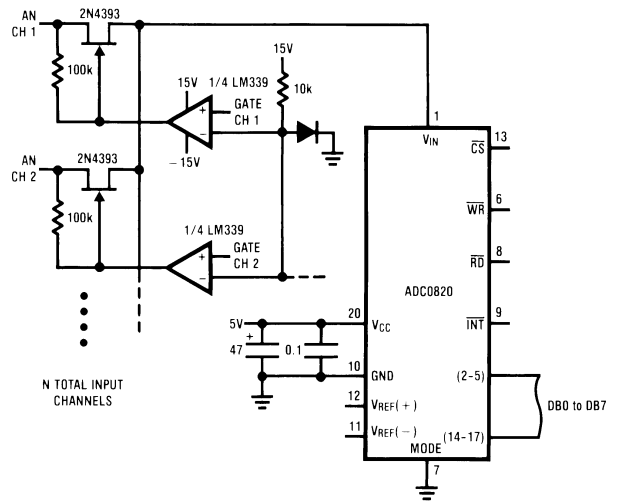
Telecom A/D Converter



00550128

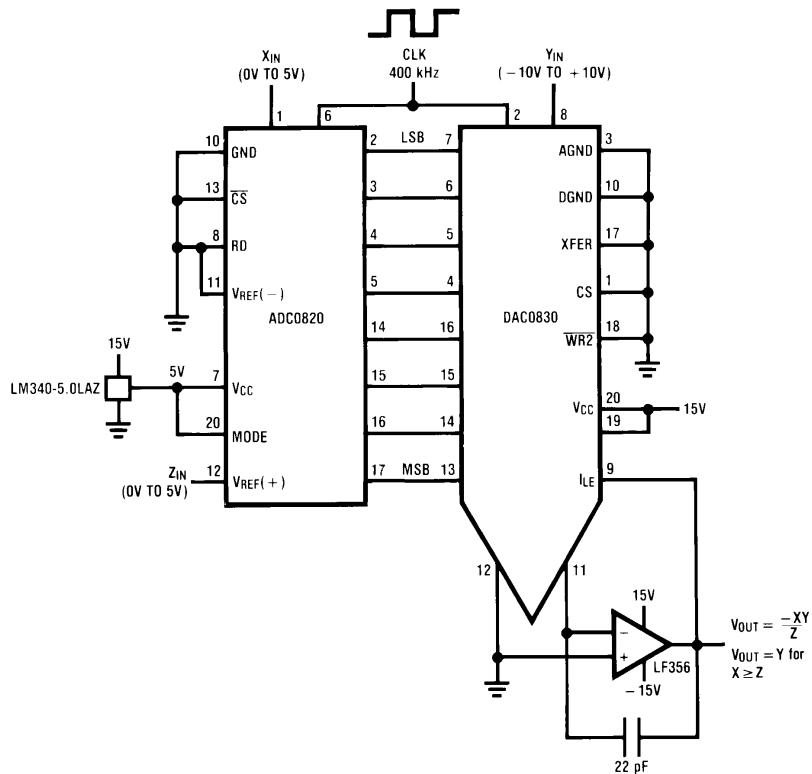
- V_{IN} = 3 kHz max \pm 4V_P
- No track-and-hold needed
- Low power consumption

Multiple Input Channels



00550129

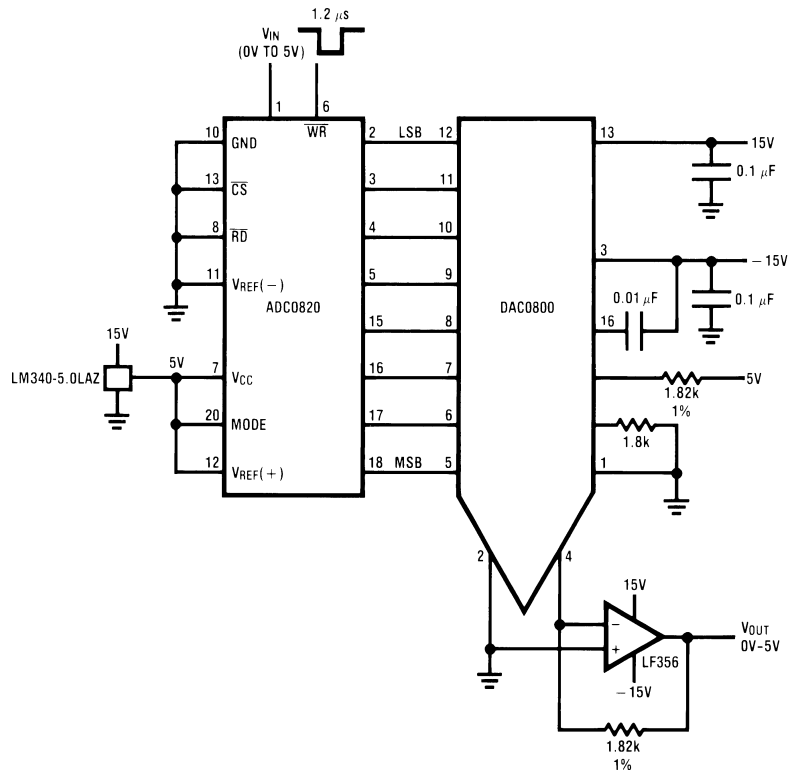
8-Bit 2-Quadrant Analog Multiplier



00550130

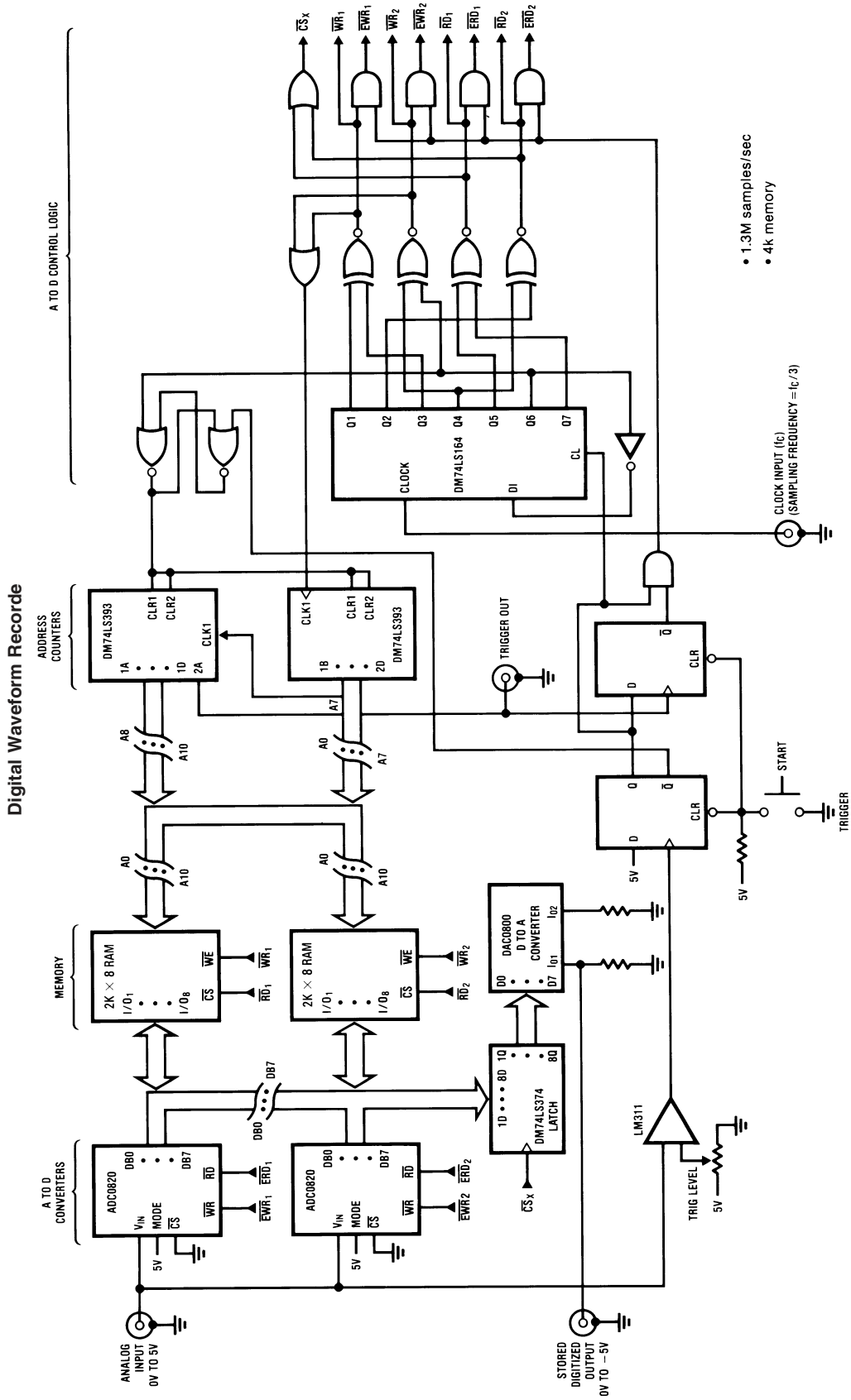
3.0 Typical Applications (Continued)

Fast Infinite Sample-and-Hold



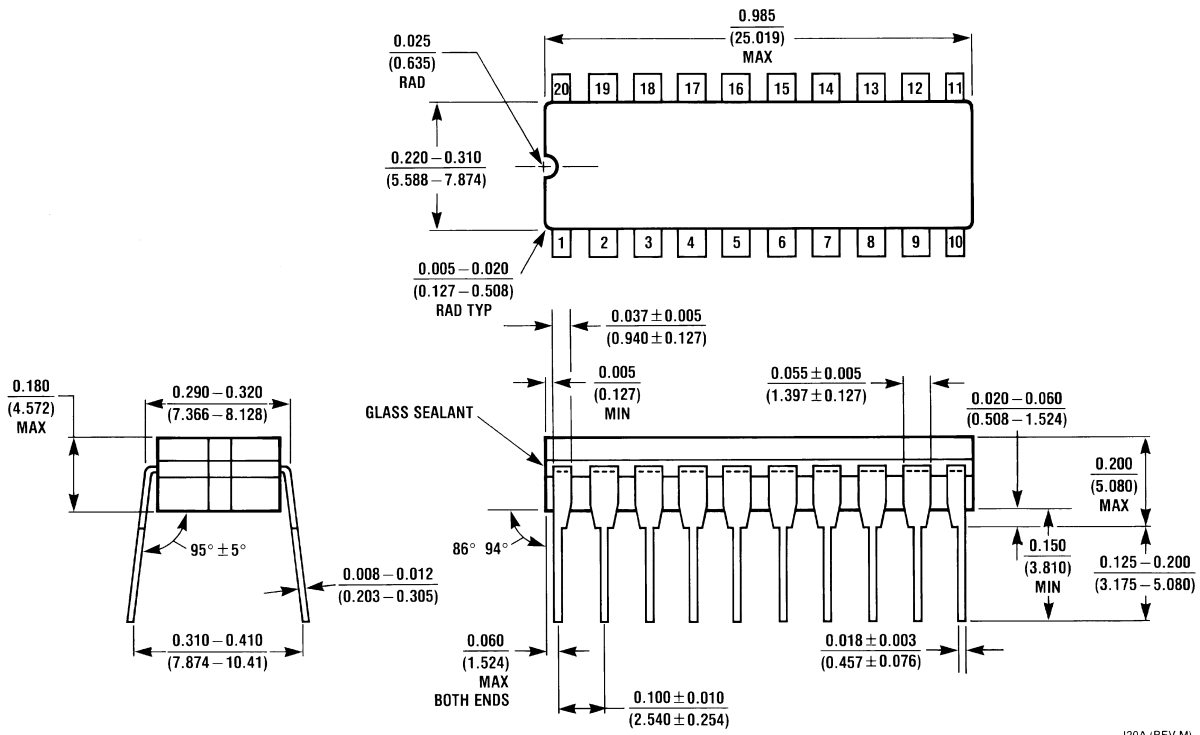
00550131

3.0 Typical Applications (Continued)



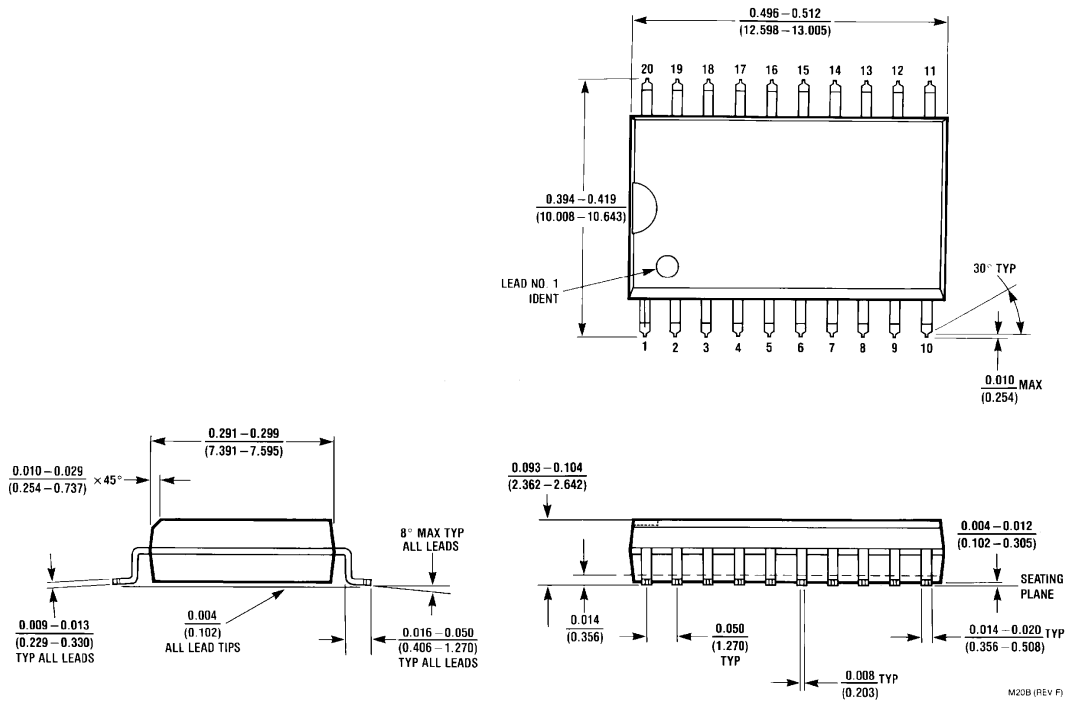
00550132

Physical Dimensions inches (millimeters) unless otherwise noted



J20A (REV M)

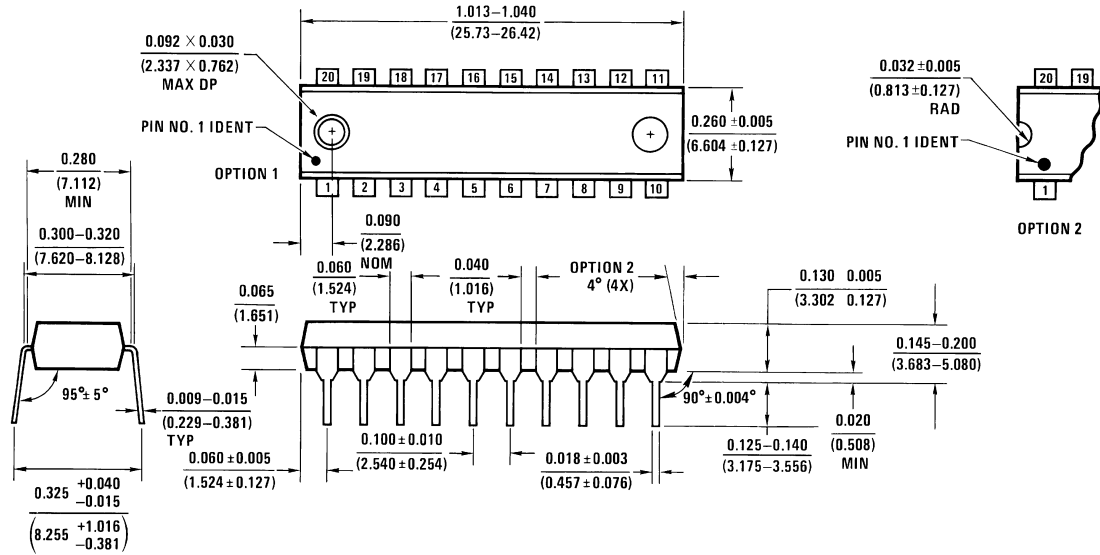
Hermetic Dual-In-Line Package (J)
Order Number ADC0820CCJ
NS Package Number J20A



M20B (REV F)

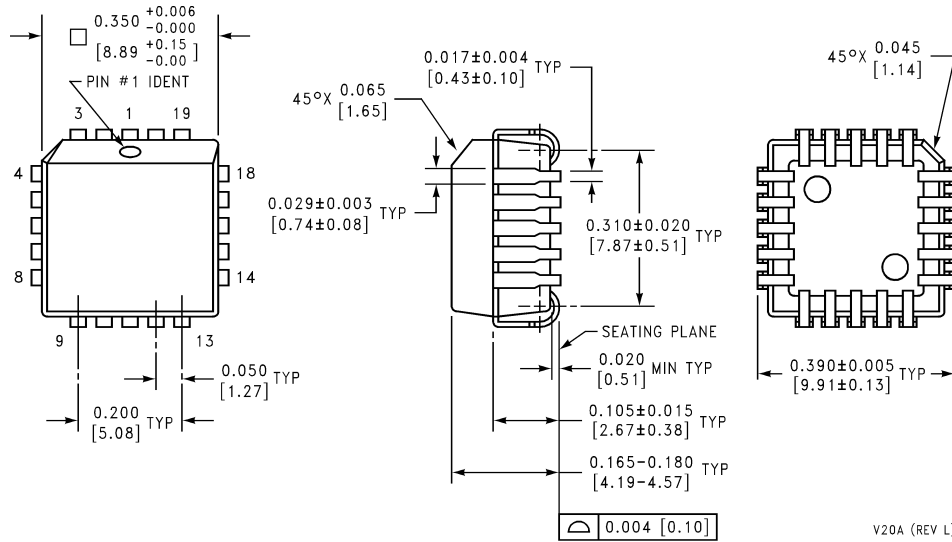
SO Package (M)
Order Number ADC0820BCWM, ADC0820CCWM or ADC0820CIWM
NS Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

Molded Dual-In-Line Package (N)
Order Number ADC0820BCN or ADC0820CCN
NS Package Number N20A



V20A (REV L)

Molded Chip Carrier Package (V)
Order Number ADC0820BCV
NS Package Number V20A

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