Outline

1. DSP project info
2. Analog-to-digital converters
3. Digital-to-analog converters
4. 2-dimensional register memory
Reminder: Project proposal is due Friday, October 9, 2009 by 5pm.
→ Lab book extensions possible.

Budget: $250 for project.

Basic guideline for project proposal (also see Project Guidelines document):
You must convince your reader that your design concept will work well enough that it deserves to be funded. This means that your design has reached the point that you can draw up a budget, and the basic design algorithm has been worked out. *Your proposal must include a budget which is as specific as possible and an expected timeline … circuit schematics are helpful.*

Free parts: Surplus parts from last year’s project will be available on a first-come-first-serve basis during the Wednesday, October 14, 2009 lab period.
As physicists, we know that:

- We live in an **analog** world of continuously varying signals.
- Almost all physical quantities (observables) are continuous in nature.

As electronics designers, we know that:

- Digital electronics is very **powerful**, **cheap**, and relatively **easy** to design (at least compared to analog circuits).
- Digital electronics only works with **digital signals**.

**THEREFORE …**

If we’re ever going to make anything useful, we need to find a way to convert (or approximate) an ANALOG signal to (by) a sequence of digital-binary numbers, and vice versa.
Algorithm: At each clock cycle, round your analog voltage to the nearest digital value.

→ The size of a digital step is defined by $V_{\text{ref}}/2^n$ for an n-bit converter.
**THEOREM:**

A continuous-time finite bandwidth signal can be exactly reconstructed from its samples if the sampling frequency is greater than 2 times the signal bandwidth B, where B is largest (non-zero) frequency component of the signal.

F=2B is referred to as the Nyquist frequency (the lowest possible sampling frequency).

**Practical Considerations:**

- Any finite duration signal has B → +∞, so exact mathematical application of the theorem is impossible.

- The theorem indicates the frequency scale that one should use in order to usefully sample a signal → always use a sampling rate which is greater than twice the highest frequency component of “reasonable amplitude”.
The fastest (and most expensive) n-bit ADCs use $2^{n-1}$ comparators to determine which of the $2^n$ numbers the analog input is closest to.

8-bit ADC: 255 comparators.

12-bit ADC: 4096 comparators

In general, higher bit resolution results in a slower ADC (and more expensive).

Most digital oscilloscopes use an 8-bit ADC.
In order to keep the number of comparators small, it holds the input voltage, and converts it in steps:

- Converts the upper four bits with a 4-bit ADC.
- Converts the digitized value back into an analog value with a Digital-to-Analog Converter (DAC).
- Subtracts this from the input to generate the smaller, difference voltage.
- Finally, it uses a 2\textsuperscript{nd} 4-bit ADC to convert the lower 4-bits.

The entire process takes less than 800 ns when operating off the internal timing of the ADC0820 (RD mode) and about 150 ns for a TLC5510A (20 MHz clock).
ADC0820: Half-Flash ADC (II)

[figure from the National Semiconductor ADC0820 datasheet]
# ADC0820: Half-Flash ADC (III)

## Functional Table

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN</td>
<td>Analog input; range GND ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>2-5</td>
<td>DB0-DB3</td>
<td>TRI-STATE data outputs; bit 0 (LSB) to bit 3</td>
</tr>
</tbody>
</table>
| 6   | WR / RDY   | **WR-RD Mode** - WR: With CS low, the conversion is started on the falling edge of WR.  
          **RD Mode** - RDY: RDY will go low after the falling edge of CS; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch. |
| 7   | MODE       | Select mode: LOW = RD Mode       HIGH = WR-RD Mode                       |
| 8   | RD         | **WR-RD Mode**  
          With CS low, the TRI-STATE data outputs (DB0-DB7) will be activated when RD goes low.  
          **RD Mode**  
          With CS low, the conversion will start with RD going LOW; also RD will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and INT going low indicates the completion of the conversion. |
| 9   | INT        | INT going LOW indicates that the conversion is completed and the data result is in the output latch. INT is reset by rising edge on RD or CS. |
| 11  | $V_{REF(-)}$ | Bottom of resistor ladder; range: GND ≤ $V_{REF(-)}$ ≤ $V_{REF(+)}$     |
| 12  | $V_{REF(+)}$ | Top of resistor ladder; range: $V_{REF(-)}$ ≤ $V_{REF(+)}$ ≤ VCC         |
| 13  | CS         | CS must be low for the RD or WR to be recognized.                        |
| 14-17 | DB4-7      | TRI-STATE data output—bits 4-7                                           |
| 18  | OFL        | Overflow—If the analog input is higher than the $V_{REF(+)}$, OFL will be LOW at the end of conversion. Can be used to cascade. |
In RD mode, the RD# line going LOW initiates the conversion.

When the conversion is complete, the INT# line goes LOW & the data is latched into output buffers.

The output buffers will be put in a Z state when WR# goes LOW until the INT# line goes LOW.

[figure from the National Semiconductor ADC0820 datasheet]
In RD mode, the RD# line going LOW initiates the conversion.

When the conversion is complete, the INT# line goes LOW & the data is latched into output buffers.

The output buffers will be put in a Z state when WR# goes LOW until the INT# line goes LOW.

[figure from the National Semiconductor ADC0820 datasheet]
TLC5510A: Basic Operation

Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>20, 21</td>
<td>Analog ground</td>
<td></td>
</tr>
<tr>
<td>ANALOG IN</td>
<td>19</td>
<td>I</td>
<td>Analog input</td>
</tr>
<tr>
<td>CLK</td>
<td>12</td>
<td>I</td>
<td>Clock input</td>
</tr>
<tr>
<td>DGND</td>
<td>2, 24</td>
<td>Digital ground</td>
<td></td>
</tr>
<tr>
<td>D1–D8</td>
<td>3–10</td>
<td>O</td>
<td>Digital data out. D1 = LSB, D8 = MSB</td>
</tr>
<tr>
<td>OE</td>
<td>1</td>
<td>I</td>
<td>Output enable. When OE = low, data is enabled. When OE = high, D1–D8 is in high-impedance state.</td>
</tr>
<tr>
<td>VDDA</td>
<td>14, 15, 18</td>
<td>I</td>
<td>Analog supply voltage</td>
</tr>
<tr>
<td>VDDD</td>
<td>11, 13</td>
<td>I</td>
<td>Digital supply voltage</td>
</tr>
<tr>
<td>REFB</td>
<td>23</td>
<td>I</td>
<td>Reference voltage in bottom</td>
</tr>
<tr>
<td>REFBS</td>
<td>22</td>
<td>Reference voltage in bottom. When using the TLC5510 internal voltage divider to generate a nominal 2-V reference, REFBS is shorted to REFB (see Figure 3). When using the TLC5510A, REFBS is connected to ground.</td>
<td></td>
</tr>
<tr>
<td>REFT</td>
<td>17</td>
<td>I</td>
<td>Reference voltage in top</td>
</tr>
<tr>
<td>REFTS</td>
<td>16</td>
<td>Reference voltage in top. When using the TLC5510 internal voltage divider to generate a nominal 2-V reference, REFTS is shorted to REFT (see Figure 3). When using the TLC5510A, REFTS is connected to VDDA.</td>
<td></td>
</tr>
</tbody>
</table>
APPLICATION INFORMATION

The following notes are design recommendations that should be used with the device.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are connected internally, the ground lead in must be kept as noise free as possible. A good method to use is twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts when additional logic devices are used. The AGND and DGND terminals of the device should be tied to the analog ground plane.
- \( V_{DDA} \) to AGND and \( V_{DDD} \) to DGND should be decoupled with 1-\( \mu \)F and 0.01-\( \mu \)F capacitors, respectively, and placed as close as possible to the affected device terminals. A ceramic-chip capacitor is recommended for the 0.01-\( \mu \)F capacitor. Care should be exercised to ensure a solid noise-free ground connection for the analog and digital ground terminals.
- \( V_{DDA} \), AGND, and ANALOG IN should be shielded from the higher frequency terminals, CLK and D0–D7. When possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 \( \Omega \) or less within the analog frequency range of interest.

[Texas Instruments TLC5510 datasheet (2003)]
A Digital-to-Analog Converter (DAC) is used to convert a digital signal into an analog voltage.

**A DAC is useful for:**

- Generating a voltage from a computer, microprocessor, or FPGA that will then control part of an experiment.
- Producing a digitally synthesized waveform (triangle, sine, or more complex).
- Converting digital music to sound, etc …

  (the CD standard is 16-bits at 44.1 KHz)

DACs are generally much faster than ADCs for a same bit resolution.
It’s easy to make the DAC output voltages.

Look from the right-hand side

- 2 parallel resistors
- Each with a value of $2R$
R-2R resistor ladder (I)

- It’s easy to make the DAC output voltages.

- Look from the right-hand side
  - 2 parallel resistors
  - Each with a value of 2R
Continuing farther to the left, we find that the effective resistance to ground is \( R \) at every dot on the top line.
The ladder acts like a series of voltage dividers that reduces the voltage by an additional factor of 2 at each $R$-$2R$ junction.

V decreases by half at each connection point along the top rail.

Thus each output voltage is related to the input voltage by a power of two.
We can generate an analog voltage by adding together the voltages represented by the various stages in the ladder.

If we sum the ladder outputs based on a simple a binary representation in switches then we have a DAC.

[figure from the *Art of Electronics* (2nd edition, 1999) by P. Horowitz and W. Hill, p. 616]
We can generate an analog voltage by adding together the voltages represented by the various stages in the ladder.

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We can generate an analog voltage by adding together the voltages represented by the various stages in the ladder.

If we sum the ladder outputs based on a simple a binary representation in switches then we have a DAC.
A real DAC: the TLC7524

[figure from Texas Instruments TLC7524 datasheet]
The data on the digital inputs is sent to the analog output when WR goes LOW.

When WR is HIGH, the digital inputs and analog output remain latched to their present values.

[figure from Texas Instruments TLC7524 datasheet]
ADC $\rightarrow$ DAC
Analog-to-Analog
2-dimensional registers with Quartus II

```verilog
module TwoD_Register(clock, output_signal);

    input clock; // input clock at 50 MHz
    output reg [7:0] output_signal; // output 8-bit binary number sequence

    reg [25:0] frequency_counter; // frequency counter used to convert 50 MHz clock to 1 Hz clock
    reg [5:0] i; // 5-bit (integers: 0-63) counter/register for addressing memory

    // Simultaneously Declare and Load the data file "data" into 2-d register memory on FPGA
    // This "(* ... *)" code is compiler specific to Quartus II (it is not universal Verilog).
    // The 2-d register memory consists of 30 words which are 8-bits long each.
    (* ram_init_file = "File_with_Data.mif" *) reg [7:0] Register_2D [0:29];

    // initialize 1-d registers

    initial
        begin
            i = 5'b00000;
            frequency_counter = 26'b00000000000000000000000000;
        end
```
2-dimensional registers with Quartus II

```verilog
// This module produces a sequence of 8-bit binary numbers
// with a period of 1 second (based on a 50.0 MHz clock).
module TwoD_Register(clock,output_signal);
    input clock;    // input clock at 50 MHz
    output reg [7:0] output_signal;    // output 8-bit binary number sequence

    reg [25:0] frequency_counter;    // frequency counter used to convert 50 MHz clock to 1 Hz clock
    reg [5:0] i;    // 5-bit (integer: 0-31) counter/register for addressing memory

// Simultaneously Declare and Load the data file "data" into 2-d register memory on FPGA
// This "(* ... *)" code is compiler specific to Quartus II (it is not universal Verilog).
// The 2-d register memory consists of 30 words which are 8-bits long each.
    (*) ram_init_file = "File_with_Data.mif" *) reg [7:0] Register_2D [0:29];

// initialize 1-d registers
    initial
        begin
            i = 5'b00000;
            frequency_counter = 26'b000000000000000000000000000;
        end
```

Declare 2-d register &
Initialize with data in file.
Using a 2-d Register in Verilog

```verilog
// This 50 MHz clock counter counts up to 50e6 in 1 seconds and then resets
// and increases in the "i" counter by 1 ("i" clock is effectively 1 Hz).
always@(posedge clock)
begin

    // increase 50 MHz frequency_counter by 1.
    frequency_counter <= frequency_counter + 1;

    // if "frequency_counter" is equal to 50 million,
    // then reset frequency_counter to ZERO
    // and send the 8-bit word corresponding to Register_2D[i] to the output
    // and increase the "i" counter by ONE.
    if (frequency_counter == 26'b10111110101111000010000000) begin
        frequency_counter <= 26'b000000000000000000000000;
        output_signal <= Register_2D[i];
        i <= i + 5'b00001;
        if (i == 5'b10000) i <= 5'b00000; // reset "i" counter to ZERO if it becomes 32.
    end
endmodule
```
Using a 2-d Register in Verilog

Reads the 8-bit word at address “i” of “Register_2D” and sends it to the 8-bit 1-d register “output_signal”.

```verilog
// This 50 MHz clock counter counts up to 50e6 in 1 seconds and then resets
// and increases in the "i" counter by 1 ("i" clock is effectively 1 Hz).
always@(posedge clock)
begin

    // increase 50 MHz frequency_counter by 1.
    frequency_counter <= frequency_counter + 1;

    // if "frequency_counter" is equal to 50 million,
    // then reset frequency_counter to ZERO
    // and send the 8-bit word corresponding to Register_2D[i] to the output
    // and increase the "i" counter by ONE.
    if (frequency_counter == 26'b10111110101111000010000000)
    begin
        frequency_counter <= 26'b00000000000000000000000000;
        output_signal <= Register_2D[i];
        i <= i + 3'b000;
        if (i == 5'b10000) i <= 5'b00000; // reset "i" counter to ZERO if it becomes 32.
    end
endmodule
```
You can write the file yourself or ...

<table>
<thead>
<tr>
<th>CONTENT</th>
<th>BEGIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 :</td>
<td>00000001;</td>
</tr>
<tr>
<td>1 :</td>
<td>00000010;</td>
</tr>
<tr>
<td>2 :</td>
<td>00000100;</td>
</tr>
<tr>
<td>3 :</td>
<td>00001000;</td>
</tr>
<tr>
<td>4 :</td>
<td>00010000;</td>
</tr>
<tr>
<td>5 :</td>
<td>00100000;</td>
</tr>
<tr>
<td>6 :</td>
<td>01000000;</td>
</tr>
<tr>
<td>7 :</td>
<td>10000000;</td>
</tr>
<tr>
<td>8 :</td>
<td>11000000;</td>
</tr>
<tr>
<td>9 :</td>
<td>10100000;</td>
</tr>
<tr>
<td>10 :</td>
<td>10010000;</td>
</tr>
<tr>
<td>11 :</td>
<td>10001000;</td>
</tr>
<tr>
<td>12 :</td>
<td>10000100;</td>
</tr>
<tr>
<td>13 :</td>
<td>10000010;</td>
</tr>
<tr>
<td>14 :</td>
<td>10000001;</td>
</tr>
<tr>
<td>15 :</td>
<td>10000011;</td>
</tr>
<tr>
<td>16 :</td>
<td>10000101;</td>
</tr>
<tr>
<td>17 :</td>
<td>10001001;</td>
</tr>
<tr>
<td>18 :</td>
<td>10010001;</td>
</tr>
<tr>
<td>19 :</td>
<td>10100001;</td>
</tr>
<tr>
<td>20 :</td>
<td>11000001;</td>
</tr>
<tr>
<td>21 :</td>
<td>11100001;</td>
</tr>
<tr>
<td>22 :</td>
<td>11010001;</td>
</tr>
<tr>
<td>23 :</td>
<td>11001001;</td>
</tr>
<tr>
<td>24 :</td>
<td>11000101;</td>
</tr>
<tr>
<td>25 :</td>
<td>11000011;</td>
</tr>
<tr>
<td>26 :</td>
<td>11000111;</td>
</tr>
<tr>
<td>27 :</td>
<td>11010111;</td>
</tr>
<tr>
<td>28 :</td>
<td>11010111;</td>
</tr>
<tr>
<td>29 :</td>
<td>11100011;</td>
</tr>
</tbody>
</table>

END;
You can use Quartus II to generate the file using the Memory Editor:

Select: New File
→ Other Files
→ Memory Initialization File
# Memory Initialization File Editor

![Memory Initialization File Editor](image.png)

<table>
<thead>
<tr>
<th>Addr</th>
<th>+0</th>
<th>+1</th>
<th>+2</th>
<th>+3</th>
<th>+4</th>
<th>+5</th>
<th>+6</th>
<th>+7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00000001</td>
<td>00000010</td>
<td>00001000</td>
<td>00010000</td>
<td>00100000</td>
<td>01000000</td>
<td>10000000</td>
<td>10000000</td>
</tr>
<tr>
<td>8</td>
<td>11000000</td>
<td>10100000</td>
<td>10010000</td>
<td>10001000</td>
<td>10000100</td>
<td>10000010</td>
<td>10000001</td>
<td>10000001</td>
</tr>
<tr>
<td>16</td>
<td>10000101</td>
<td>10010001</td>
<td>10010001</td>
<td>10100001</td>
<td>11000001</td>
<td>11100001</td>
<td>11010001</td>
<td>11010001</td>
</tr>
<tr>
<td>24</td>
<td>11000101</td>
<td>11000011</td>
<td>11000111</td>
<td>11001011</td>
<td>11010011</td>
<td>11100011</td>
<td>11100011</td>
<td>11100011</td>
</tr>
</tbody>
</table>

- **word memory address**
- **8-bit word** (enter by hand)

**Right-click** to enter type memory information: integer, hexadecimal, binary, etc …
If your memory space is not very large, the compiler will automatically choose to implement your Verilog circuit with D-type flip-flops of the Logic Elements. You can force the compiler to use the dedicated FPGA memory:

Assignments > Settings >
Logic Element or RAM memory?

If your memory space is not very large, the compiler will automatically choose to implement your Verilog circuit with D-type flip-flops of the Logic Elements.

You can force the compiler to use the dedicated FPGA memory:

Assignments > Settings >

---

### More Analysis & Synthesis Settings

Specify the settings for the logic options in your project. Assignments made to an individual node or entity in the Assignment Editor will override the option settings in this dialog box.

**Option:**
- **Name:** Allow Any RAM Size For Recognition
- **Setting:** Off
- **Description:** Allows the Compiler to infer RAMs of any size, even if they don't meet the current minimum requirements.

### Existing option settings:

- **Name:** Add Pass-Through Logic to Inferred RAMs
  - **Setting:** On
- **Name:** Allow Any RAM Size For Recognition
  - **Setting:** Off
- **Name:** Allow Any ROM Size For Recognition
  - **Setting:** Off
- **Name:** Allow Any Shift Register Size For Recognition
  - **Setting:** Off
- **Name:** Allow Synchronous Control Signals
  - **Setting:** Off
- **Name:** Auto Carry Chains
  - **Setting:** On
- **Name:** Auto Clock Enable Replacement
  - **Setting:** On
- **Name:** Auto Open-Drain Pins
  - **Setting:** On
- **Name:** Auto RAM Replacement
  - **Setting:** On
- **Name:** Auto RAM to Logic Cell Conversion
  - **Setting:** Off
- **Name:** Auto Resource Sharing
  - **Setting:** Off
- **Name:** Auto ROM Replacement
  - **Setting:** Off
- **Name:** Auto Shift Register Replacement
  - **Setting:** Auto

---

} turn ON
Check compiler report for memory usage:

<table>
<thead>
<tr>
<th>Flow Status</th>
<th>Successful - Mon Oct 22 03:03:49 2007</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quartus II Version</td>
<td>7.1 Build 156 04/30/2007 SJ Web Edition</td>
</tr>
<tr>
<td>Revision Name</td>
<td>TwoD_Register</td>
</tr>
<tr>
<td>Top-level Entity Name</td>
<td>TwoD_Register</td>
</tr>
<tr>
<td>Family</td>
<td>Cyclone II</td>
</tr>
<tr>
<td>Device</td>
<td>EP2C35F672C6</td>
</tr>
<tr>
<td>Timing Models</td>
<td>Final</td>
</tr>
<tr>
<td>Met timing requirements</td>
<td>N/A</td>
</tr>
<tr>
<td>Total logic elements</td>
<td>55</td>
</tr>
<tr>
<td>Total combinational functions</td>
<td>55</td>
</tr>
<tr>
<td>Dedicated logic registers</td>
<td>31</td>
</tr>
<tr>
<td>Total registers</td>
<td>31</td>
</tr>
<tr>
<td>Total pins</td>
<td>9</td>
</tr>
<tr>
<td>Total virtual pins</td>
<td>0</td>
</tr>
<tr>
<td>Total memory bits</td>
<td>256</td>
</tr>
<tr>
<td>Embedded Multiplier 9-bit elements</td>
<td>0</td>
</tr>
<tr>
<td>Total PLLs</td>
<td>0</td>
</tr>
</tbody>
</table>