Potential roughness suppression in a RF AC Zeeman atom chip trap

William Miyahira[a] and Seth Aubin[a]

[a]Department of Physics, William & Mary, Williamsburg, VA, USA

ABSTRACT

Trapping and manipulating ultracold atoms through the use of atom chips offers the ability to engineer complex electromagnetic field geometries in a compact form factor. One of the primary limitations hindering their use is trap potential roughness which arises as a result of defects in the atom chip wires when atoms are brought close to the chip. This roughness can play a limiting role in atom interferometry and strong 1D confinement experiments. We present an initial experimental demonstration of atom chip potential roughness suppression using radio-frequency (RF) AC Zeeman (ACZ) potentials on an atom chip. Using ∼20 MHz RF magnetic near-fields from the chip to target intra-manifold transitions in the ^{87}Rb ground state, we trap atoms in a spin-dependent ACZ potential. We compare the axial trapping potential for atoms in comparable 2-wire DC and AC Zeeman traps and show evidence of roughness suppression in the AC trap.

Keywords: Ultracold atoms, atom chip traps, potential roughness, AC Zeeman

1. INTRODUCTION

Atom chips offer experimenters the ability to produce and control ultracold atomic gases in a compact physics package. These chips can feature complex wire structures for engineering unique field structures for trapping and manipulating atoms using the DC Zeeman (DCZ) effect. One of the primary attributes plaguing the more widespread adoption of atom chips is trap potential roughness. This effect arises due to microscopic defects in the micro-fabricated atom chip wires and acts to fragment the ultracold atom cloud. The potential roughness increases in the vicinity of the chip, limiting how close the atoms can be brought to the chip, and can affect experiments in atom interferometry and strong 1-D confinement of ultracold gases, for example. Previously, it has been shown that modulating the currents in the atom chip at a few tens of kHz can time-average out roughness effects in a DCZ trap.[1] Additionally, graphene has been proposed as a wire conductor[2] for limiting roughness.

In an alternate approach, we find that this potential roughness is significantly suppressed by using RF currents on an atom chip to generate spin-dependent trapping potentials based on the AC Zeeman (ACZ) effect. Radio frequency[3] and microwave[4] near-fields on an atom chip have been demonstrated to generate spin-specific forces using the ACZ effect. Recently, an ACZ trap using ∼20 MHz RF currents to target the intra-manifold transitions within the hyperfine manifolds of the ground state of ^{87}Rb has been demonstrated on an atom chip in our group.[5] On the theory side, a trap based on the ACZ effect has been shown to suppress potential roughness effects by up to $\sim 10^4$ compared to a traditional DCZ trap for the same trap height and frequency.[6] In this work, we show the first experimental demonstration of potential roughness suppression in an ACZ chip trap. We utilize a 2-wire trapping scheme to generate comparable DCZ and ACZ traps and show qualitative suppression in the ACZ trap compared to the DCZ trap.

Further author information: (Send correspondence to S.A.)
W.M.: E-mail: whmiyahira@wm.edu
S.A.: E-mail: saaubi@wm.edu

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2. SUPPRESSION IN THE AC ZEEMAN TRAP

2.1 Origins of Potential Roughness

Roughness in the harmonic trapping potential generated by the atom chip arises from defects in the chip wires, such as variations in the trace's bulk conductivity or indents on the edge of the wire (Figure 1(a)). When these kinds of defects are present in the atom chip wires, the current through the wire deviates from its average straight line path to accommodate these imperfections. When this happens, a local magnetic field component in the axial direction along the length of the trace is generated ($B_{||}$ in Figure 1(b)). Now, in the case of a DCZ trap, in addition to the harmonic axial potential provided by endcap wires on the atom chip there exists regions of local axial confinement which can act to fragment the ultracold atom cloud.

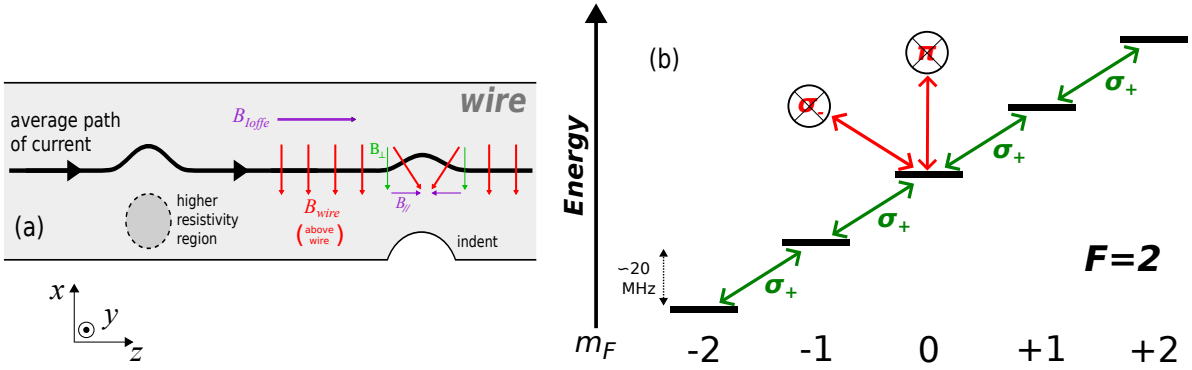

Figure 1. Potential roughenss suppression physics. (a) Defects in the atom chip wire (gray), such as non-uniform conductivity or an indent in the edge of the wire, causes the current in the trace (black line) to deviate from its straight line path. When the current in the chip wire strays from its path due to a defect, forming an angle θ with the z-axis, magnetic fields are generated along the axial (z) direction that add linearly to the external B_{ioffe} field, forming a local minimum in the trapping field resulting in regions of local axial confinement in the trapping potential. Figure adapted from Du et al.[6] (b) Energy level diagram of the F=2 hyperfine manifold in the $5S_{1/2}$ ^{87}Rb ground state. The energy separation between Zeeman sublevels, labeled by m_F, is ~20 MHz, set by the background DC magnetic field. When a RF magnetic field is applied, these states couple via the AC Zeeman effect. In this case, only σ_+ transitions are possible, while σ_- and π transitions do not exist. Thus, any π polarized fields generated by chip wire defects ($B_{||,RF}$ in (a)) will not affect the ACZ trapping potential.

2.2 Suppression Via Selection Rules

When a magnetic field is applied to the atoms, they feel an energy shift given by the Zeeman effect, which couples the magnetic moment of the atom to the field, $\Delta E_{Zeeman} = -\vec{\mu} \cdot \vec{B}$, where $\vec{B}$ can either be a DC or RF magnetic field. In the traditional DCZ trap scheme, the trapping potential ΔE_{DCZ} is proportional to $|\vec{B}_{DC}(\vec{r})|$, i.e. $\Delta E_{DCZ} = \langle m_F| - \vec{\mu} \cdot \vec{B}_{DC}|m_F\rangle$. In the ACZ scheme, however, the trapping potential is proportional to the Rabi frequency coupling the m_F states, $\Omega_{ACZ}(\vec{r})$, which depends on the polarization of the applied magnetic field,[7] i.e. $\Delta E_{ACZ} = \langle m_F| - \vec{\mu} \cdot \vec{B}_{RF}|m_F^{'}\rangle$ (with $m_F \neq m_F^{'}$). Any local axial fields generated by chip wire defects ($B_{||}$ in Figure 2(a)) will therefore add vectoraly into the DC trapping potential, and will drive π polarized transitions (Δm_F=0) in the ACZ trap potential. In our experiments, we target atomic transitions between m_F states in the F=2 hyperfine manifold of the the $5S_{1/2}$ ^{87}Rb ground state (See Figure 2 (b)). The Rabi frequency dictating the coupling between these states in an AC magnetic field only operates on σ_+ transitions (i.e. it is insensitive to σ_- and π transitions). Thus, in the ACZ trap, the local axial fields from chip wire defects which drive π transitions will not affect the trapping potential, suppressing the effects of potential roughness. We note that the same suppression scheme can be realized by driving microwave σ_+ inter-manifold transitions between the F=1 and F=2 hyperfine manifolds. In this case, by applying a sufficiently large background DC field, π transitions generated by the roughness can be be effectively suppressed by making them far off-resonance.

In addition to the selection rule suppression, we also note that at high enough frequency (the 6.8 GHz ground state hyperfine splitting of ^{87}Rb, for example) the AC skin effect will also act to suppress potential

roughness. For example, in the case of a region of higher or lower conductivity, DC currents will be forced to alter their path around this area. However, the skin effect will cause AC currents to hug the edges of the chip wire, effectively ignoring this region.[6] This additional suppression could be realized in an atom chip based on broadband microwave structures such as microstrips.[7]

3. EXPERIMENT

3.1 Experimental Setup

We prepare a sample of ultracold ^{87}Rb atoms using a dual vacuum chamber apparatus.[8] We begin by trapping approximately 10^8-10^9 ^{87}Rb atoms in a standard magneto-optical trap (MOT). After a brief optical molasses sequence for further cooling, the atoms are optically pumped into the $|F = 2, m_F = 2\rangle$ hyperfine state of the $5S_{1/2}$ ground state. The atoms are then transported via a purely magnetic trap into a Z-wire atom chip trap in a second chamber, where we trap $\sim 10^6$ atoms. Further cooling on the chip is done through forced RF evaporation down to a few μK. Once cooled, we adiabatically transfer $\sim 10^5$ atoms into either the 2-wire DCZ or ACZ trap. We then hold the atoms in the 2-wire trap for a few hundred ms to reduce any thermal motion from the transfer.

3.1.1 Two-Wire Traps

To explore the proposed roughness suppression we utilize a 2-wire scheme (parallel Z and U shaped wires on the chip, 100 μm separation center-to-center) for both the DC and AC Zeeman traps. Figure 2 shows a diagram of the trapping scheme for both types of trap.

DCZ Trap: In the DCZ trap the currents in the two parallel chip wires are in opposite directions. By applying an external bias field in the vertical (y) direction, we can cancel out the field generated by the wires and trap the low-field seeking atoms in the $|2, 2\rangle$ state. This bias field can be used to adjust the vertical position of the trap, while the relative current in each wire acts to adjust the horizontal position with some effect on the vertical as well. We operate our DC trap using 400 and 325 mA in the chip wires, respectively, with a 9.35 G bias field, resulting in a measured trap height of 76 ± 4 μm. We apply a gradient push coil (B_{push} in Figure 2) along the axial direction to align the trap axially with the ACZ trap.

ACZ Trap: For the ACZ trap we use the same two chip wires, this time putting $\sim$200 mW of RF current at 20.58 MHz through each, operating on the σ_+ RF intra-manifold transitions.[5] We estimate that the atomic resonance is around 20.85 MHz, placing us a few hundred kHz below resonance and trapping primarily the $|2, 2\rangle$ state. The chip wires have a relative phase difference of 114°. This phase controls the height of the trap and is adjusted to match the DC trap, measured to be 78 ± 5 μm. We implement a gradient push coil (B_{push} in Figure 2) along the axial direction to limit sloshing when the atoms are transferred into the two-wire ACZ trap.

3.1.2 Matching Trap Parameters

We took care in matching the horizontal and vertical (trap height) position as well as the radial trap frequency in accordance with previous theoretical work.[6]

To measure the position of the atoms below the chip we use a dark-ground imaging technique to generate a "dark spot" in our absorption images. The vertical position of the atoms from the chip is then half the distance between the atoms and the dark spot. We utilise a short time-of-flight (0.25 ms) to ensure minimal movement of the atoms prior to imaging. The error bar is a standard deviation of about 15 images for each trap. The measured trap height is within an errorbar of the calculated trap height for the DC trap using 1-D wires.

We take care to also match the radial trapping frequency of the two traps. After trapping the atoms in either the DCZ or ACZ trap, we give them a push using a chip wire to initiate oscillations in the trap. We image the atoms after different hold times and extract the position of the atoms as a function of time. This data can be fit with an exponentially decaying sinusoid to extract the horizontal and vertical trap frequencies. We choose to match the average of the two, $(\omega_x + \omega_y)/2$, for each trap, which is what is reported in Figure 2.

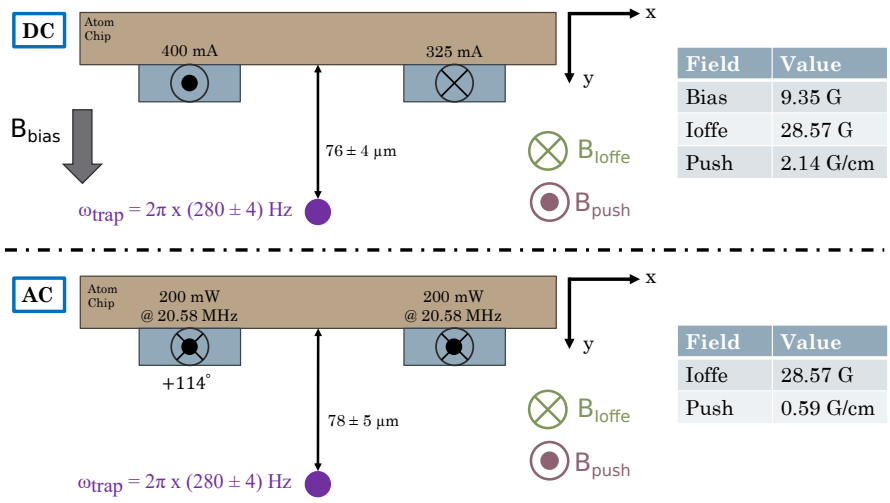

Figure 2. Experimental setup for the potential roughness suppression experiments. Current (either DC or RF) is sent through two parallel chip wires to generate the trapping potential. In the case of the DCZ trap (top), a vertical bias field, B_{bias} is used to cancel out the magnetic field from the chip wires, creating a trap for low-field seeking states. For the ACZ trap (bottom), no external bias field is applied. A magnetic field in the z-direction, B_{ioffe}, sets the quantization axis and the Zeeman sublevel splitting. Additionally, a gradient push coil is used to both align the two traps axially as well as minimize axial oscillations when loading into the 2-wire trap.

3.2 Results

The main results of this work are shown in Figure 3 . We average over 75 absorption images of atoms in each trap. The axial trapping potential can be extracted from the number density using the equation[8]

$$U(z) = -k_B T[\ln(n(z))], \tag{1}$$

where $n(z)$ is the atom number density, k_B is Boltzmann's constant, T is the temperature of the atoms, and $\lambda = h/\sqrt{2\pi m_{Rb} k_B T}$ is the deBroglie wavelength where m_{Rb} is the mass of the ^{87}Rb atom. Temperature measurements are taken before and after the axial data (i.e. data in Figure 3) using traditional time-of-flight ballistic expansion of the atom cloud.

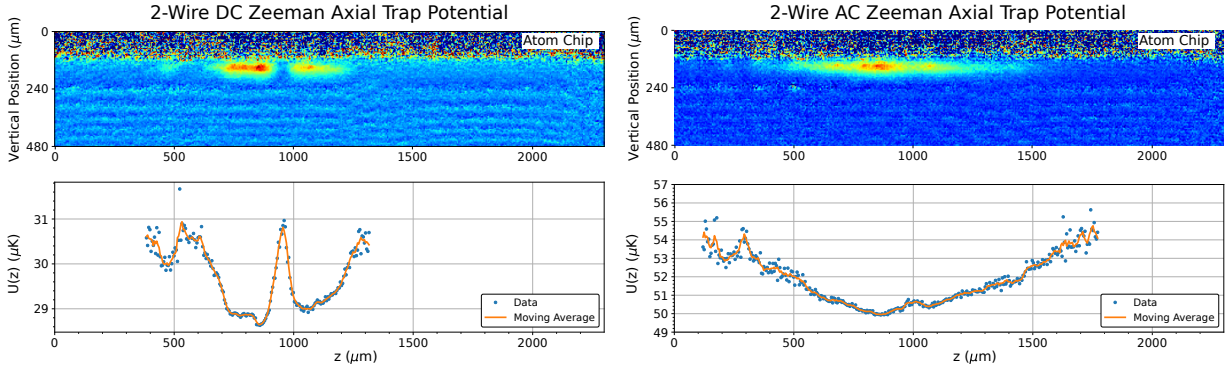

Figure 3. Extracted axial trapping potentials for the 2-wire DC (left) and ACZ (right) chip traps for the setups and parameters in Figure 2 after a 1 ms time-of-flight. The data is averaged over 75 shots (top images), and uses Equation 1 to extract the potential in μK as a function of axial position (bottom images). The orange curves in the bottom plots are a five point moving average. The temperatures of the atoms are $T_{DCZ} = 0.99$ μK and $T_{ACZ} = 1.68$ μK, respectively.

Looking at the data in Figure 3 we see a clear suppression of potential roughness in the AC Zeeman trap. In the DCZ trap we can make out about three distinct roughness features at roughly z=500, 800, and 950 μm of varying size, indicating varying defect sizes. We also see in the absorption images that the DCZ trap features obvious fragmenting of the atom cloud with local areas of confinement in addition to the overarching harmonic potential, resulting in a fragmented atom cloud. In the ACZ trap we observe a much smoother potential compared to the DC case. Comparing the size of the roughness feature at $\sim$1,000 μm (950 μm for the DCZ trap), we see a suppression factor of $\sim$4 in the ACZ trap. The suppression factor is theorized to be larger for smaller defect sizes,[6] so we may need to lower the temperature of the atoms in the ACZ trap to better resolve the suppression for small bumps in the DC trapping potential. We also note that the axial (z) position of the roughness bumps at $\sim$1,000 μm is offset between the two traps, consistent with theory.[6]

4. CONCLUSION AND OUTLOOK

We have experimentally demonstrated the suppression of atom chip potential roughness using an ACZ trap. Using a two-wire trapping scheme for both DCZ and ACZ potentials we see clear qualitative evidence of suppression in the ACZ trap for the same trap height and frequency. We are also interested in characterizing further the ACZ trap potential roughness for different detunings (RF frequencies), RF powers, and trap heights. This will act as the first look into the roughness exhibited using this novel trapping scheme and will help inform the viability or limitations of future experiments due to the potential roughness. Future ACZ atom chip traps using two or three microstrips[7] will allow for a broadband atom chip, giving access to hyperfine transitions in multiple atomic species (^{87}Rb, ^{39}K, ^{40}K, ^{41}K), the use of a microwave lattice for axial confinement and translation, and added roughness suppression through the AC skin effect.

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