

Chapter 7: AC Transistor Amplifiers

The transistor amplifiers that we built two weeks ago had some serious problems for use in AC signals. The most serious was that there was a “dead region” where small signals did not turn on the transistor. So, if your signal was smaller than 0.6 V, or if it went negative, the transistor didn’t conduct and the amplifier did not work.

Design goals for an AC amplifier

Before moving on to making a better AC amplifier, let’s define some useful terms. We define the *output range* to be the range of possible output voltages. We refer to the maximum and minimum output voltages as the *rail voltages* and the *output swing* is the difference between the rail voltages. The *input range* is the range of input voltages that produce outputs which are not at either rail voltage.

Our goal in designing an AC amplifier is to get an input range and output range which is symmetric around zero and ensure that there is not a dead region. To do this we need make sure that the transistor is in conduction for all of our input range. How does this work? We do it by adding an offset voltage to the input to make sure the voltage presented to the transistor’s base with no input signal, the resting or *quiescent voltage*, is well above ground.

Now that you understand capacitors it is pretty easy to see how to add and subtract an offset voltage to a signal, at least for AC signals. From here on, you will design transistor circuits with a bias network. This bias network is simply a voltage divider that is connected to the input. Its job is to insure that the output stays at approximately half the supply voltage for small input signals. Then, the output voltage can vary over a wide range (positive and negative) while always keeping the transistor conducting.

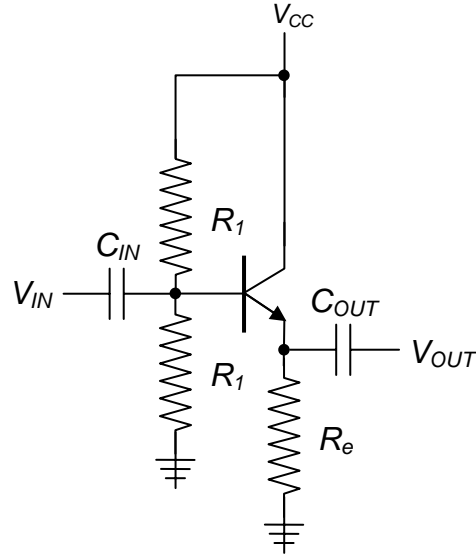
The trick to make this work is to separate these quiescent voltages and currents from the input and output signals. To do this, you will use blocking capacitors to isolate the input and the output. If you connect an AC input to a capacitor, it will not pass any DC offset voltages but it does pass the fast AC signals. Similarly, an output blocking capacitor will pass the fast signal while keeping the quiescent (resting) voltage from the amplifier from disturbing whatever comes next. This is shown schematically in the first figure (next page).

Some Design Basics

This week we are going to redesign our emitter follower and inverting amplifier to use bias networks. To help you with your design, we will make a step by step list for designing each of these basic transistor circuits.

Here are a couple initial design decisions we will make

- You will begin by determining the quiescent (DC, no signal) current through the collector. You usually want the quiescent current to be larger than any current you will use to drive a load. A quiescent current of 1 mA is typical, and we will use that in our example designs.
- We will also use a single +15 V power supply to power the collector (the *common collector voltage* or V_{CC}) for both circuits.
- We need to be careful about loading the different stages of this amplifier. The transistor's base current will load the output of our bias voltage divider. To bias the base, we need a stiff voltage divider (i.e. low impedance). Our rule of thumb for design dividers was to have a factor of 10 difference in impedance at each stage. In this case, we will typically use biasing resistors that are smaller than the emitter resistors by a factor of 10 or so (the two equal biasing resistors will then have a parallel impedance of $R_e/20$).



AC Emitter Follower

Design steps for the emitter follower would proceed as follows:

1. To have the maximum symmetric range of output voltages we would like our quiescent base voltage to be half of the (15 V) supply voltage. So, we will use a 1:1 input voltage divider. This means that both biasing resistors will be the same.
2. We then choose the emitter resistor. The quiescent voltage at the emitter is a diode drop below the voltage in the middle of the bias network (i.e. $V_{cc}/2$ if we have a 1:1 divider). This is roughly +7 V in our case. To get our design quiescent current, the emitter resistor must be

$$R_e = V_e/I_e = 7 \text{ V} / 1 \text{ mA} = 7 \text{ k}\Omega.$$

Let's use the standard 6.8 K Ω . It is close enough.

3. To bias the base we want a stiff voltage divider (i.e. low impedance), therefore we want to use resistors that are smaller than the base-emitter-ground impedance ($Z_b=V_b/I_b \sim 750 \text{ k}\Omega$) by a factor of 10 or so. For this example, we will choose two 75 k Ω resistors for this divider.
4. Remember to AC couple (via capacitors) the input and output. The exact values are not particularly important, though you should remember that you making a biased high-pass RC filter. Values around 0.1 μF are typical if you want $f_{3dB} \sim 15 \text{ Hz}$, but you can use what you have as long as it is not too small.

Common Emitter (Inverting) Amplifier

In this circuit, we need to know the quiescent current and the desired gain. Let's assume a gain of -5 and a 1mA quiescent current for this example.

1. In this circuit we want the quiescent output (at the collector) to be set roughly halfway between the power supply and the ground for maximum output voltage swing. For $I_c = 1 \text{ mA}$,

$$R_c = V_c / I_c \approx 7 \text{ V} / 1 \text{ mA} = 7 \text{ k}\Omega.$$

We will use a standard resistor of about this value (e.g. $R_c = 6.8 \text{ k}\Omega$) as we did for the follower.

2. The emitter resistor can be determined by the desired gain. Previously we saw that

$$\text{Gain} = -R_c / R_e$$

In our case we want a gain of 5 so we chose $R_e = 1.35 \text{ k}\Omega$. We will approximate this by a standard $1.5 \text{ k}\Omega$ resistor. Note that with this choice, the emitter quiescent voltage will be given by the voltage drop across the emitter resistor

$$I_c R_e = 1.5 \text{ V}.$$

3. The tricky part is to design the bias network for this circuit. Since we know the emitter voltage, the output of the bias network (i.e. the base voltage) is just a diode drop higher than the emitter voltage. Therefore the bias resistors must be set to give

$$\begin{aligned} V_2 &= V_e + 0.6 \text{ V} \\ &= 1.5 \text{ V} + 0.6 \text{ V} \\ &= 2.1 \text{ V}. \end{aligned}$$

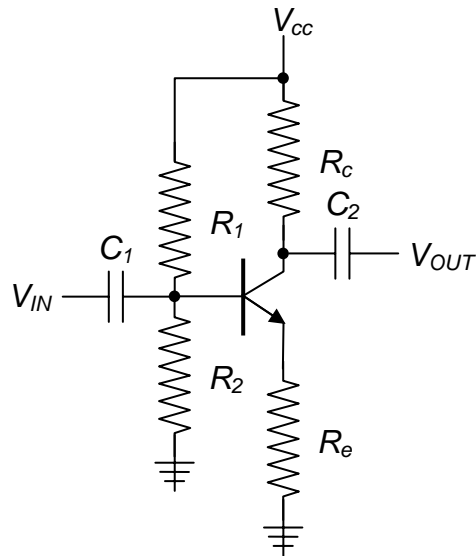
This is the drop across the lower of the two bias resistors. The other has a drop of

$$\begin{aligned} V_1 &= V_{cc} - V_2 \\ &= 15 \text{ V} - 2.1 \text{ V} \\ &= 12.9 \text{ V} \end{aligned}$$

The bias network's output impedance must be high enough to keep this bias up even when loaded. We will select the smaller bias resistor to be 10 times the smaller of the transistor's resistors (the smaller of R_e or R_c). Thus, our smaller bias resistor will be

$$R_2 = 10R_e = 15 \text{ k}\Omega.$$

and we can now get the other resistor since we know the ratio of voltage drops across the two resistors:



Chapter 7: AC Transistor Amplifiers

$$I_{Bias} = V_1 / R_1 = V_2 / R_2 .$$

Therefore,

$$R_1 = (V_1 / V_2) R_2 = (12.9V / 2.1V) 15k\Omega = 92k\Omega$$

We will approximate this by a standard 100 k Ω resistor.

4. Remember to AC couple the input and output with capacitors. The values are not particularly important.

Design Exercises

Design Exercise 6-1: Design an AC emitter follower with a 1.5 mA quiescent current. Remember that you can approximate the resistor values by picking the nearest standard values. Please show any approximations when they are employed.

Design Exercise 6-2: Design an AC inverting amplifier with a 0.2 mA quiescent current and a gain of 15.

Design Exercise 6-3: Calculate what happens in the hybrid emitter-follower circuit below. What is the current through the load resistor? What does this circuit do? Is it a “good” design?

