# MidTerm Results and Overall Performance

#### Midterm:

Average: 69%.

High Score: 94%.

Lab Books: The lab books have been improving ... mostly (write down as much as you can).

 $\rightarrow$  You should expect to do more analysis at home after the lab.

Lab Report: Quality has been decreasing ... mostly. You need to invest more care and effort into your lab reports.

# **Transistors II: AC transistor Amplifiers**

#### **Emitter-Follower Amplifier Summary**

#### **Pros:**

- Power/Current Gain.
  Speaker got louder.
- Simple.
- Moderate input impedance.
- > Does not depend on  $\beta$ .

Cons:

- Requires a DC bias.
  - → Signal cannot be negative !
  - → Signal must be larger than 0.6 V.
- Cannot provide Voltage Gain.
- Significant power consumption.

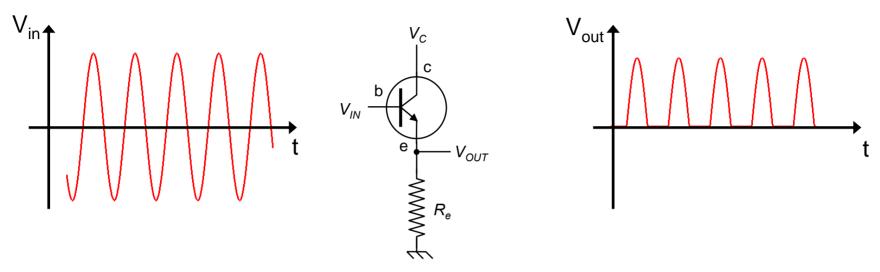
#### **The DC bias problem**

There are 2 simple solution to the DC bias problem:

> Push-Pull amplifier.

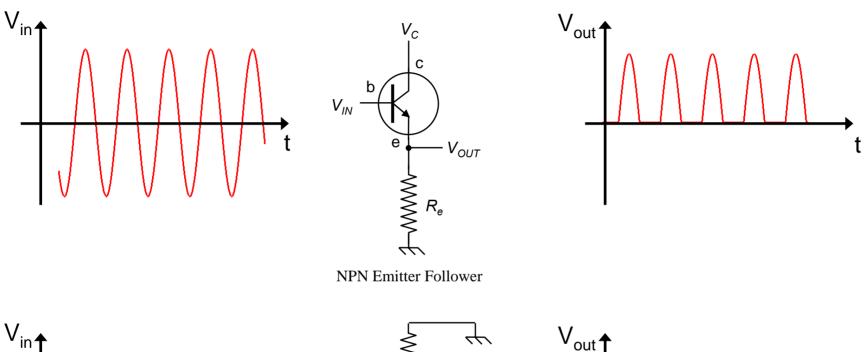
#### AC-coupled biased-amplifier

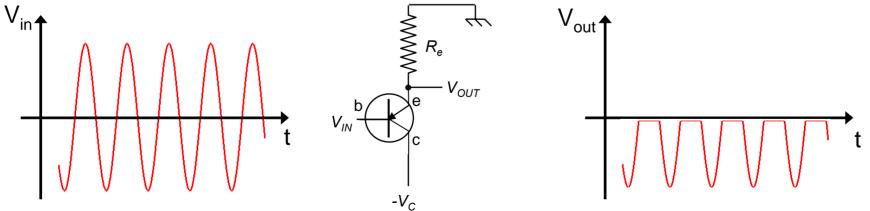
#### **Push-Pull BJT Amplifier (I)**



NPN Emitter Follower

## **Push-Pull BJT Amplifier (I)**

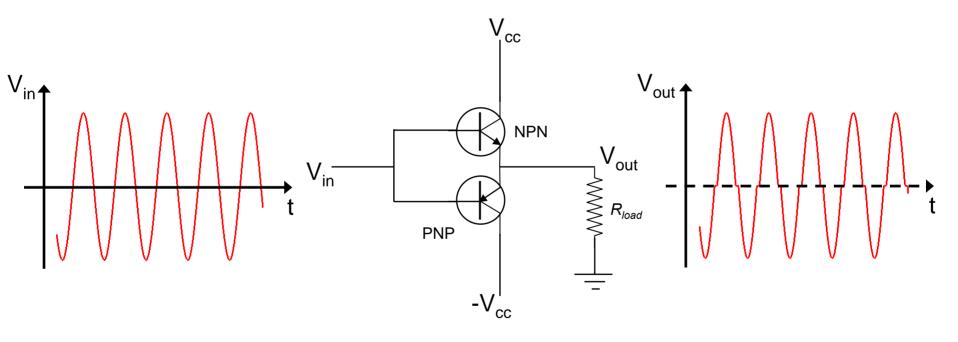




PNP Emitter Follower

## **Push-Pull BJT Amplifier (II)**

#### **Combine both circuits:**

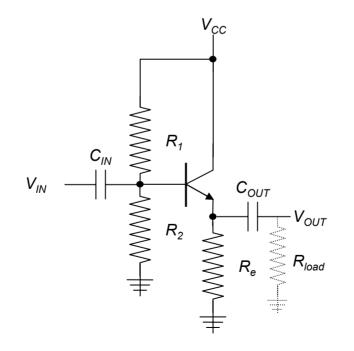


Push-Pull BJT Amplifier No DC bias required

### **AC-coupled Biased-Amplifier**

AC-couple the input and output signals with capacitors (i.e. high-pass RC filters)

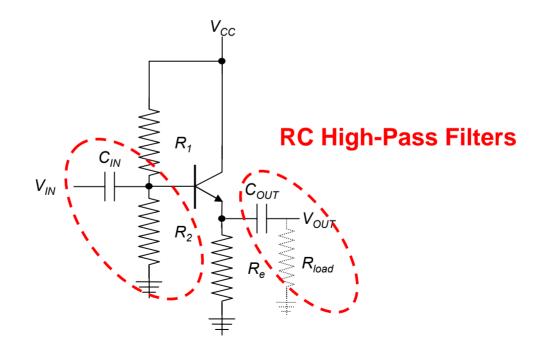
DC-bias the input with a voltage divider.



## **AC-coupled Biased-Amplifier**

AC-couple the input and output signals with capacitors (i.e. high-pass RC filters)

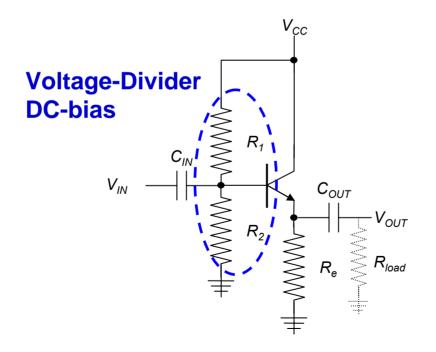
 $\succ$  DC-bias the input with a voltage divider.



## **AC-coupled Biased-Amplifier**

 AC-couple the input and output signals with capacitors (i.e. high-pass RC filters)

DC-bias the input with a voltage divider.



# **AC Transistor Amplifier Design**

#### 4 rules:

Choose a *quiescent collector current* (no load current) which is at least 10x larger than load current.

> Choose  $V_{out, DC}$  in the middle of the supply voltage range for maximum signal voltage amplitude.

▷ Choose the DC-bias such that  $V_{collector} > V_{base}$  (NPN) to avoid saturation, and  $V_{base} \sim V_{emitter} + 0.6$ .

> Make sure that the voltage divider DC-bias and the transistor don't load each other (i.e.  $I_{base}$  10x smaller than  $I_{voltage-divider}$ ).