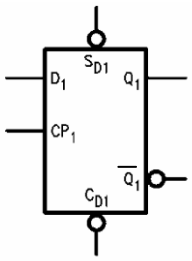
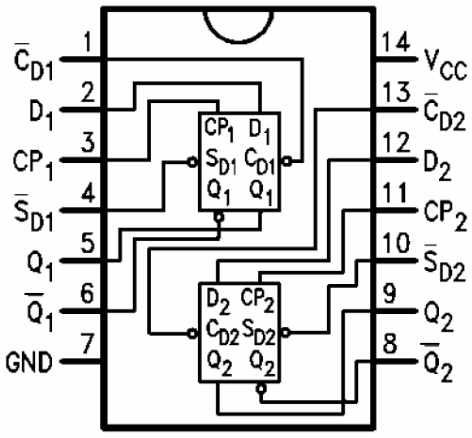
Laboratory 3: Flip-Flops

1. Use two 74LS00 NAND gates to create an “SR latch”. Use slider switches as inputs. Verify its truth table. The standard notation for a *Q* output that does not change is Q_0. The “0” subscript implies that the current value is the same as the previous value. Now use a switch to “trigger” the latch as it falls from high to low (a *falling edge*). You should be able to see the switch output bouncing between the two states from the sliders if you slide one SLOWLY. Verify that putting switch through a latch “debounces” the switch.
2. Use two more 74LS00 NANDs and an inverter to create a clocked D-type latch. Verify its truth table.
3. Make another clocked SR latch from 74LS00 gates. Combine the two latches to make a master/slave edge-triggered flip-flop. Verify its truth table. Measure the propagation delay between the clock edge and when the data appears on *Q*. Measure the rise and fall times of the transitions on the output. Estimate the gate delay of a single TTL NAND. What do you think will be the maximum clock frequency that your device can handle? Explain.
4. Use a 74LS74 D-type edge-triggered flip-flop, construct a truth table, and compare its performance to your previous devices (e.g. the propagation delay). Note that this chip also has *S* and *R* inputs so you can set the state to a specific value. Also note the negative true nature of these inputs.

D-Type Edge-Triggered Flip-Flop

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$





Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs