Laboratory 5: Counters and registers

This week you will use an 8-bit shift register to convert data (i.e. a series of ones and zeros) between serial and parallel formats. You will also use counters and multiplexers on the DE2 board to create a frequency counter with kHz resolution.

1. Set-up an 8-bit shift-register circuit with a 74LS164 chip. Use logic switches in combination with either a very slow function generator clock or a debounced switch clock. Measure the input and clock with a slow oscilloscope time setting and verify that the parallel outputs are what they should be. Output the data from the serial out port (i.e. the last parallel out channel) and verify that the data is properly saved and outputted.

2. Use Quartus II and the FPGA on the DE2 development board to convert a 15-bit binary number from the switches on the DE2 (SW[0-12]) to a 5-digit decimal representation which is displayed on the LED "Hex" displays (HEX0[0-6], HEX1[0-6], HEX2[0-6], HEX3[0-6], HEX4[0-6]). The unused displays should be turned off.
   Test your binary-to-decimal converter with a few numbers to make sure that it works properly

3. Use Quartus II and the FPGA on the DE2 development board to count the number of positive edge triggers on an input pin for 100 ms (and every 100 ms after that) and display the result in little-endian binary format with red and green LEDs of the DE2 (LEDR[0-17] and LEDG[0-8]). Your counter should be able to measure the frequency of the 27 MHz clock attached to pin PIN_D13 (i.e. CLOCK_27).
   What frequency do you measure for the 27 MHz clock? Also test your counter with the function generator.

4. Combine the Verilog modules of your Quartus II projects from parts 2 and 3 to create a frequency counter which counts the number of positive edge triggers on an input pin for 100 ms and displays the frequency in kHz in decimal representation on the "Hex" displays. The resolution of the display does not have to be better than 1 kHz (you do not have to round up or down), though a higher precision of 1 Hz is acceptable (for enthusiasts).
   What frequency do you measure for the 27 MHz clock? Also test your counter with the function generator.
   Note: Your "Hex display" Verilog code of part 2 may require more than the 15-bits of input for part 4, however part 4 still requires only 5 "Hex" displays.