Fall 2008 **Syllabus**

Electronics II – Physics 351: Digital Electronics for Physicists

## Instructors

**Prof. Seth Aubin**
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Lab: room 15 (basement, next to machine shop), tel: 1-3532
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Austin Ziltz
Office: room 243, tel: 1-3570

Office hours:

| | |
|---|---|
| Tuesday | 4-5 pm (Aubin) |
| Monday | 3-4 pm (Ziltz) |

## Course Objectives

The primary purpose of this course is to teach you how to design both basic and advanced digital electronic circuits for digital logic, signal acquisition, and digital signal processing.

### *a. Topics:*

The course will cover the following to topics:

- Binary numbers, logic gates, and Karnaugh maps.
- Memory, flip-flops, and clocked latches.
- Clocks, timing, and one-shots.
- Counters, registers, and state machines.
- Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC).
- Optical and magnetic isolation.
- Field Programmable Gate Arrays (FPGA).
- Verilog language FPGA programming.
- Digital Signal Processing (DSP).

### *b. FPGAs for Physicists*

FPGAs, or Field Programmable Gate Arrays, are a type of programmable logic chip in which complex digital circuits can be programmed into a chip: the thousands of logic gates inside the chip are hard-wired to provide a compact and reliable digital circuit.

### *c. Digital Signal Processing Project*

A central component of the course is an FPGA-based digital signal processing project. The purpose of the one month team project is to help you develop practical digital circuit design skills, as well as the following more general research skills:

- Complex device design.

- Project budgeting.
- Formal project proposal writing.
- Finding, selecting, and purchasing device components.
- Device construction.
- Troubleshooting and debugging.
- Oral and web presentations of the device.

Each project team will consist of 2-3 students and will have a budget of $250 USD.

## Course Materials

***Course notes:*** There is no official textbook for the course. I will be posting introductory chapters and laboratories created specifically for the course on my website before the lecture. These chapters and labs were originally created by Prof. Jeff Nelson and Prof. Bill Cooke and have been adapted to the current course.

While there are many good electronics textbooks, I strongly recommend that you consult the following book frequently for design tips and concepts: The Art of Electronics ($2^{nd}$ Edition, 1989-1999) by P. Horowitz and W. Hill. It is available in the Physics Library under call number TK7815 .H67 1989. A copy is also available for reading in my office.

***Software:*** The course will rely heavily on the Quartus II FPGA programming software by Altera Inc, an industry standard for FPGA programming. The software package can be used to program FPGAs and to simulate almost any type of digital circuit. Advanced FPGA programming will involve the Verilog programming language which is include in the Quartus II software package. The software is available on the electronics lab computers (Small Hall, room 148) and on specific Swem library campus computers. It is strongly recommended that you install the software on your personal computer – note: required disk space is 5 GB.

## Class Format

The class hours are divided into two parts: Lecture and Lab. The lecture will be on Monday 2:00-2:50 pm in room 238, and will cover the concepts to be tested in the lab later in the week. The lab portion of the class will be held on Tuesday 2:00-4:50 pm for Physics 351-02 (14201) and Wednesday for Physics 351-01 (14200).

The labs will be open from 1:00 pm to 6:00 pm for students looking to start early or finish late. Most labs will include a design component. The designs should be prepared prior to attending lab so as to finish the lab measurements on time. The designs can prepared and refined using the Quartus II software.

## Evaluations

Your final grade for the course will be determined from the following grading weight distribution:

| | |
|---|---|
| Notebooks/Reports: | 30% |
| Quizzes/Participation: | 10% |
| DSP project: | 60% |

**Notebooks:** Your lab book should be a composition style notebook with either line or quadrangle ruling or a computation logbook. It can be obtained at most stationary stores (i.e. campus bookstore, Staples, Office Depot, etc …)

Your lab book is the primary record of your work and data. You should record everything that you do in the lab book, so that anyone (such as the instructors and yourself) can understand what you have done and measured. You should include circuit diagrams, observations, questions, answers, design considerations, measurement data, and analysis. Diagrams, data, graphs, and other notes on separate pieces of paper should be glued, taped, or stapled into the lab book. As a general rule, you cannot write too much down.

The lab book will be graded primarily on completeness and to a lesser extent on neatness (i.e. better to be complete than neat, though doing both is better yet). It should also feature a table of contents. The lab books will be turned in every weeks and returned before the next lab.

***You should enter you lab notes and data directly into the lab book. A "scratch" lab book that is neatly copied into the lab book at a later time is not appropriate and will result in a significantly reduced participation grade.***

**Lab reports:** Scientists and engineers communicate their activities and research results through short reports. Each student is required to turn in a report. The instructor will indicate which labs will require reports. You can expect to turn in two to three reports during the semester. The lab report is due by the following Monday, either in class or at my office.

The lab report should present what you did in the lab. The reports should have the following characteristics and components:

- Typed or printed.
- Short report (max 3 pages single space, but shorter is better).
- Structured with an introduction, a main body, and a conclusion.
- Measurement data should be included in tables and plots.
- All data should be analyzed and interpreted.
- Important measured numbers should include a justified error bar.

**Quizzes:** There will be occasional 5 minute quizzes at the beginning of lecture and lab to encourage you to review concepts and circuit design.

**Research Design Project:** The design project is the most important part of the course and will be graded as follows:

| | |
|---|---|
| Formal project proposal | 10% |
| Device construction | 15% |
| Device performance | 20% |
| Oral presentation of device. | 5% |
| Web presentation of device | 5% |
| Project lab book and wiki | 5% |
| **Total** | **60%** |

**Final exam:** There is no final exam for the course.

## Weekly Schedule

**Week 0: 8/25-27** **NO CLASS**

**Week 1: 9/1-3** **Digital Logic**
Class & lab: Binary numbers, logic gates, Karnaugh maps.

**Week 2: 9/8-10** **Introduction to FPGAs**
Class & lab: FPGAs, Verilog programming language, applications.

**Week 3: 9/15-17** **Memory**
Class & lab: Memory, flip-flops.

**Week 4: 9/22-24** **Timing**
Class & lab: Clocks, timing, one-shots, and counters.

**Week 5: 9/29 -10/1** **Counters and Registers**
Class & lab: Counters II and registers.

**Week 6: 10/6-8** **Analog-Digital Interfacing**
Class & lab: Analog-to-digital converters, digital-to-analog converters, digital isolation.
***Project:*** Formal project proposals are due October 10, 2008.

---------- Fall Break ----------

**Week 6.5: 10/15** Wednesday lab group jumps one week ahead
Class: No class; Lab: Project; project funds are released.

**Week 6: 10/20-22** **State Machines and/or Microprocessors**
Class & lab: State machines and sequencing.

**Week 8: 10/27-29** **Project week 1**
Class: Surface mount soldering review and machine shop training.
***Project:*** Project construction begins.

**Week 9: 11/3-5** **Project week 2**
Class: Digital signal processing.
***Lab & Project:*** Project construction continues.

**Week 10: 11/10-12** **Project week 3**
Class: Tri-state logic.
***Lab & Project:*** Project construction continues.

**Week 11: 11/17-19** **Project week 4**
Class: Ground loops and opto-isolation.
***Lab & Project:*** Project construction and debugging. Two lab sections equalize schedules.

**Week 12: 11/24-25** **Project week 5**
Class: Microprocessors on FPGAs *or* phase-lock loops.
***Lab & Project:*** Project debugging and troubleshooting.

**Week 13: 12/1-3** **Project week 6**
Class: Oral presentations and website launch.
***Lab & Project:*** Device performance testing and review.